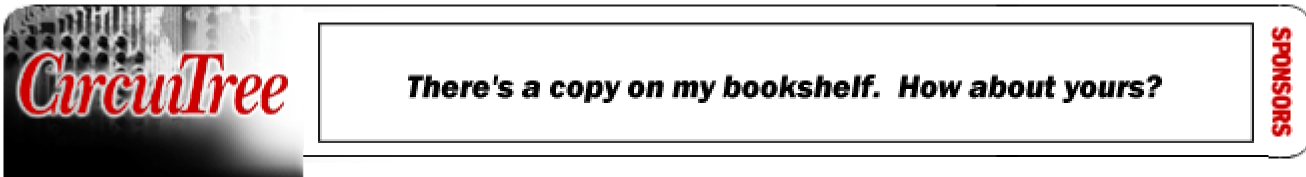

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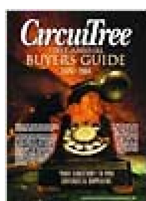
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Via Life vs. Temperature Stress Analysis of Interconnect Stress Test

Michael Freda

POSTED: 03/01/2005

Interconnect Stress Testing (IST) was developed during the 1990s as a test method for measuring plated through via and interconnect reliability in printed circuit boards. A new data analysis methodology presented here provides significant insight into plated through via reliability versus thermal stress temperature [1, 2]. This IST testing and data analysis method gives insight into the consumption of plated through via life during assembly and rework, the impact of lead-free processing versus eutectic solder, and (potentially) the ability to predict the remaining life of products in the field.

IST testing utilizes special test equipment to measure cycles to failure (CTF) on specially designed IST coupons placed on PCB fabrication panels. These IST coupons contain daisy chains of plated vias that are thermally cycled using ohmic heating (i.e., by using an internal resistance heater circuit) until failure which is defined as a 10% resistance increase of a plated via daisy chain. The IST test equipment [3] has a number of advantages, including: a quick cycle time of 5 minutes per cycle or 288 cycles per day, the ability to thermally cycle IST coupons at assembly temperatures including lead-free peak temperatures at 260°C, and the ability to obtain quantitative data on plated via CTF.

History of IST Testing at Sun

Sun's first use of IST was during the early prototype development of the SunFire™ server product line. This family of servers currently spans the range from 24 to 212 processors per system. The CPU board utilized in the SunFire™ systems has 26 layers, may use blind and buried vias, and uses mixed metallization with selective Cu/Ni/Au plating in the land grid array socket areas and HASL everywhere else. Plated hole aspect ratios range from 8:1 to 9:1 depending upon the drilled hole size selected by the PCB fab supplier. With 26 layers in an overall thickness of 2.8mm, the resulting

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stack-up has thin dielectric cores and a high resin to glass ratio.

Early prototype testing of IST coupons on the SunFire CPU boards used varying assembly precondition stresses of 0x, 3x, and 6x at 230°C followed by test to failure at 150°C. This testing showed that six assembly cycles consumes 50-80% of the via life. It was common to see POST Separation failures due to the large Z-axis CTE expansion of the high resin construction of the CPU board. The high Z-axis expansion resulted in a large shear stress on inner layer connections close to the top and bottom surface of the PWB. These issues were corrected prior to product release by reducing the resin percent and improvements in the hole metallization process.

By production release of the SunFire product line, Sun had standardized on an IST testing protocol of 6x preconditioning at 230°C, followed by test to failure up to a maximum of 500 cycles at 150°C. During early production the average CTF obtained from IST testing continued to increase due to process improvements at fabrication. Nonetheless, the PCB fab supplier that had the highest CTF average was also most prone to early life failures. In 2001 Sun started to use the Weibull distribution and a CTF criteria based on the T1% obtained from the CTF data where T1% is the predicted first failure from testing 100 IST coupons. To get acceptable CTF results on the T1% metric, the PCB fabrication supplier must have both a good process (indicated by a high characteristic life) and a consistent process (indicated by a high slope). By late 2002 Sun switched to using a lognormal distribution because it is a better fit to the data in a majority of the data analyzed and because it was a better predictor of early life failures which is Sun's primary interest.

Recently Sun started allowing some of its PCB fab suppliers to test at 230°C to failure. This change was made after extensive testing to failure at both 150°C and 230°C. Data from this testing was then used to establish the acceleration factor between 150°C and 230°C CTF data. Once the acceleration factor has been established, we used Miner's Rule [4] to predict CTF to the pre-existing baseline which used the IST testing protocol of 6x at 230°C followed by CTF at 150°C. This change was made due to the large increase in CTF over time that resulted in long test times.

A number of trends in the industry make via reliability testing increasingly important:

- Lead-free regulations. Switching to a SAC alloy (tin/silver/copper) results in a 30-35°C increase in peak assembly reflow temperatures.
- Increased signal speeds require either wider traces and thicker dielectrics, low loss laminates, or some combination of both to minimize attenuation loss. This results in either thicker PCB fabs with higher aspect ratios or a switch to new laminate materials which need to be characterized at lead-free assembly conditions.

- The use of large 2000+ pin, 1mm pitch, area array packages which require filled via in pad designs.

Test Panel Description

All data reported here comes from testing on a 450 x 600 x 4mm panel that contains 24 IST coupons of four IST coupon designs:

1. 300micron drilled hole with both PTH and POST interconnect daisy chains.

2. 350micron drilled hole with both PTH and POST interconnect daisy chains.

3. 350micron drilled hole PTH daisy chain and a 660micron drilled hole POST interconnect daisy chain.

4. 400micron drilled hole with both PTH and POST interconnect daisy chain.

Hole aspect ratios on the test panel are 13:1, 11:1, and 10:1. The panel is laid out so there are six groups of IST coupons. Within each group are four IST coupons, i.e., one of each IST coupon design. For the test results reported here three groups/panel used standard plated though holes and three groups/panel used filled vias where the process was to drill the filled vias, plate, fill, planarize, drill the non-filled vias, and then plate. It should be noted that due to the mix of filled and non-filled holes on a panel, even the non-filled vias are subjected to a different process flow than a standard panel with only non-filled vias.

Via Reliability Design of Experiments

The data that follows was obtained from testing on the PCB panel designed by Sun and PWB Interconnect Solutions described in the preceding section.

Mechanical Parameter	Measured Data	Units
Tg by TMA	171.2	°C
Z-axis CTE < Tg	24.4	PPM/°C
Z-axis CTE > Tg	197.3	PPM/°C
TMA Tg transition	151-178	°C
Z-axis expansion, 230°C	1.5	%
Z-axis expansion, 260°C	2.1	%
Tg by DMA	172	°C
Storage modulus below Tg	16,400	MPa
Storage modulus above Tg	900	MPa
DMA Tg transition	155-190	°C
Laminate Description	aromatic phenolic cured epoxy glass laminate with inert filler to lower CTE	

Table 1. Mechanical properties of the laminate material used in this DOE.

That test panel design plus material and process selections results in the

following design of experiment (DOE) conditions:

- 3 factors - Drilled hole diameters of 300micron, 350micron, and 400micron.
- 4 factors – The IST coupon designs described earlier.
- 2 factors - Filled and non-filled vias.

The IST coupons with the DOE variations above were tested to failure at 130°C, 150°C, 170°C, 230°C, and 260°C.

Data Naming Conventions

- F = IST coupons with filled vias
- N = IST coupons with non-filled via
- xxxC = IST test temperature in ^{o}C
- yyy = designates IST coupon designs where the same drilled hole diameter (yyy in micron) is used for both PTH and POST interconnect daisy chains
- 350/660 = the IST coupon design where a 350micron drilled hole diameter is used for the PTH daisy chain and a 660micron drilled hole diameter is used for the POST interconnect daisy chain

Example: F/170C/350 refers to an IST coupon design with filled vias, a 350micron drilled hole size for both the PTH and POST daisy chains, and IST testing at 170°C. In tables and graphs of IST coupon design versus temperature this name would be shortened to F/350 since the temperature will now be shown in the other axis/column.

IST Testing Conditions

The typical IST test cycle involves a linear three-minute ramp from ambient to peak temperature. When the peak temperature is reached, the heater power supply is turned off and a fan is switched on to cool the IST coupon using ambient air for two minutes. This cycle is then repeated.

For the testing at 230°C and 260°C the IST coupons where cycled from ambient to 230°C (or 260°C) until failure. For the testing at 130°C, 150°C, and 170°C the IST coupons where first cycled two times from ambient to 260°C followed by test to failure at 130°C, 150°C, or 170°C. The reasons for performing these two preconditioning cycles are:

- A high temperature exposure may effect and change the laminate

materials, not performing this preconditioning step may create misleading CTF results and...

- All assembled product receives a minimum of two assembly reflow thermal stress cycles.
- Because assembly thermal stress has a large effect on via life, performing this preconditioning shortens the CTF testing required at the lower temperatures.

Lognormal Data Analysis

	IST Testing Temperature (degrees C)				
	260°C	230°C	170°C	150°C	130°C
F/300	2.59		6.30	346	1079
F/350	4.79	7.43	63.4	233	2287
F/350/660	4.96	6.97	37.7	115	1262
F/400	7.13			215	2374
N/300	6.62			80.1	83.4
N/350	16.8	19.5	26.5	579	480
N/350/660	3.94	12.9	55.4	157	1268
N/400	15.3			284	1069

Table 2. IST CTF data for each DOE design variation versus testing temperature. Data shown is the T1% lower 90%, two sided confidence interval using a lognormal MLE analysis.

The initial data analysis was performed with Minitab release 13 using its lognormal base e MLE (maximum likelihood estimate) analysis. Results are summarized in Table 2.

Photos 1-3 show microsections taken from filled and non-filled vias. Failure analysis of vias that fail early and comparison to vias with high CTF can be very informative. For example, Photo 1 shows how the use of filled vias can lead to a change in the failure mode.

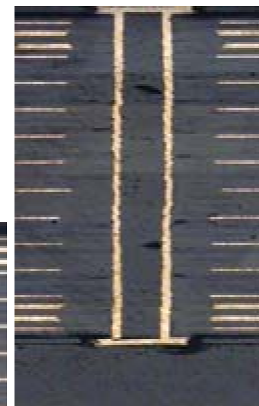
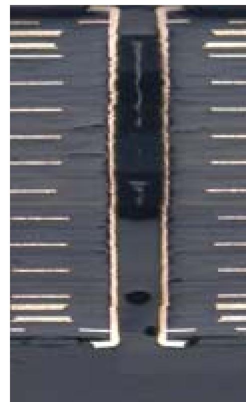


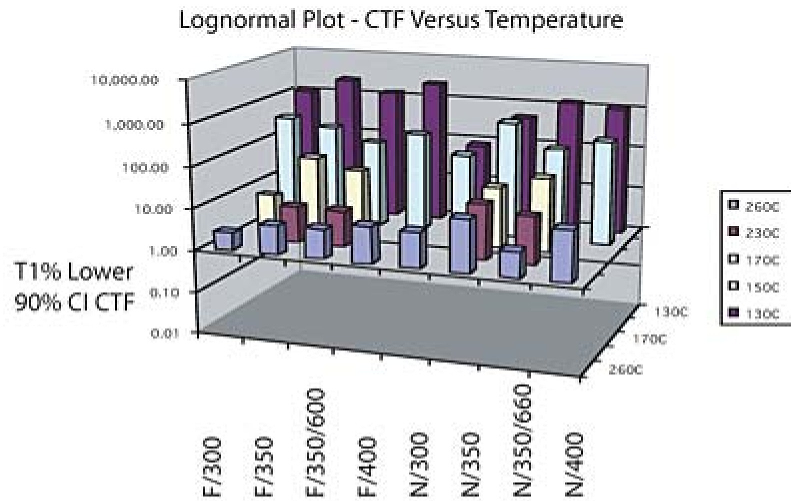
Photo 1. Microsection of a filled via from another lot (not from this DOE).

In the photo it appears the expansion rate of the fill material is too high and during thermal stress it popped off the bottom portion of the plated via cap. This failure occurred during 2x preconditioning at 260°C.



Inverse

Photo 2. Microsection of a non-filled via. Failure occurred after two preconditioning cycles at 260°C and



Graph 1. IST CTF data from Table 2 is plotted. Filled vias (F) are on the left side and Non-filled vias (N) are on the right side. Within both the Filled and Non-filled via date hole size increases going from left to right.

One of the goals of this DOE was to establish the CTF reliability of PCB fab vias versus applied thermal stress. Three temperatures were used for testing below Tg, 130°C, 150°C, and 170°C to judge if the life-stress relationship under test is a good fit to the data.

Several life-stress data analyses relationships were considered including Arrhenius, Eyring and IPL (inverse power law). IPL was selected due to its better fit and its extensive utilization in metal fatigue analysis [5]. IPL uses the temperature difference from high to low temperature extremes. In this testing the temperature induced stresses were: 108°C (130°C peak - 22°C ambient), 128°C, 148°C, 208°C, and 238°C. This represents a 37% difference between the temperature induced life-stress at 130°C (a 108°C difference) and 170°C (a 148°C difference).

The mathematical relationship for IPL is [6]:

$$L(V) = 1/KV^n \qquad \text{(eq. 1)}$$

Where:

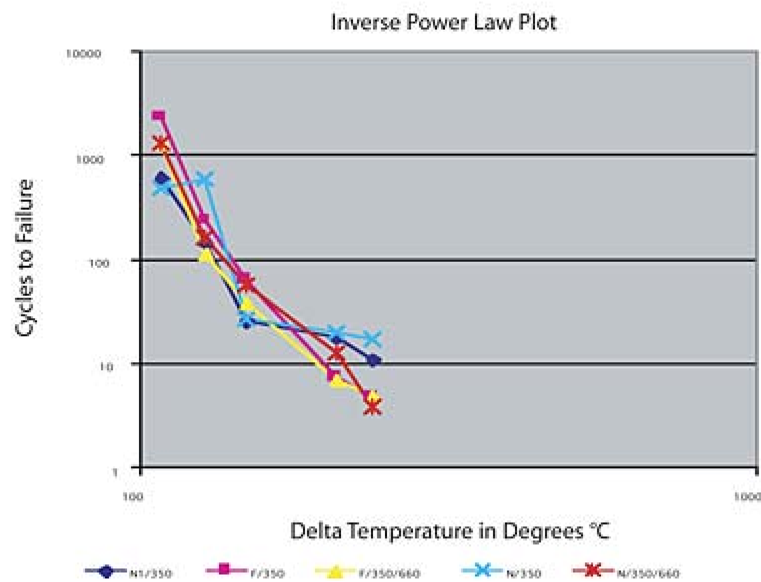
- **L** represents a quantifiable life measure, in the case IST CTF
- **V** represents the stress level, i.e., the temperature difference

between IST peak and ambient

- **K** is one of the model parameters to be determined, (K>0)
- **n** is another model parameter to be determined

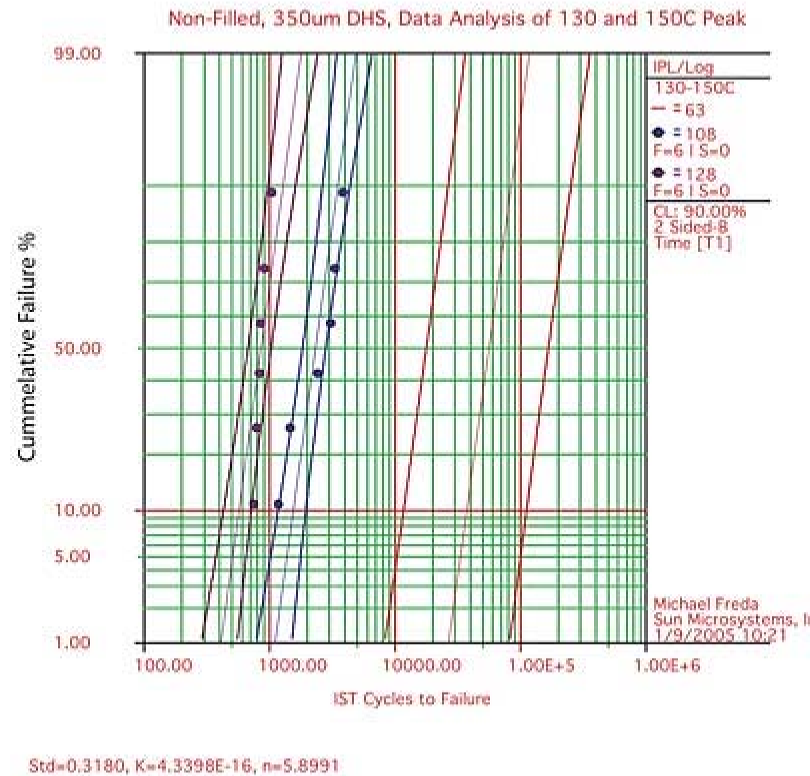
The IPL appears as a straight line when plotted on a log-log paper. The equation of the line is given by:

$$\ln(L) = -\ln(K) - n\ln(V) \quad \text{(eq. 2)}$$
$$y = c + mx \quad \text{(eq. 3)}$$



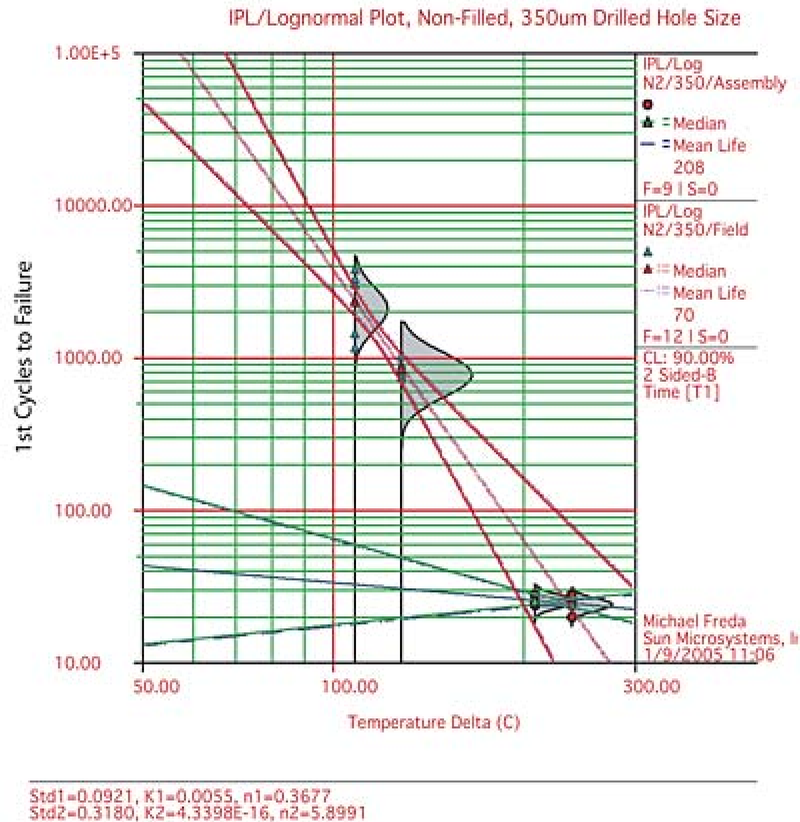
Graph 2. Log-Log plot consistent with an IPL relationship. Note the lower slope above Tg.

Graph 2 shows a Log-Log plot of five cells of the DOE that followed the expected trend and share a common 350micron drill hole size. While this spreadsheet plot is crude, it shows that a straight line, IPL life-stress relationship, does not exist over the full temperature range. As expected, the slope above Tg does not match the slope below Tg.



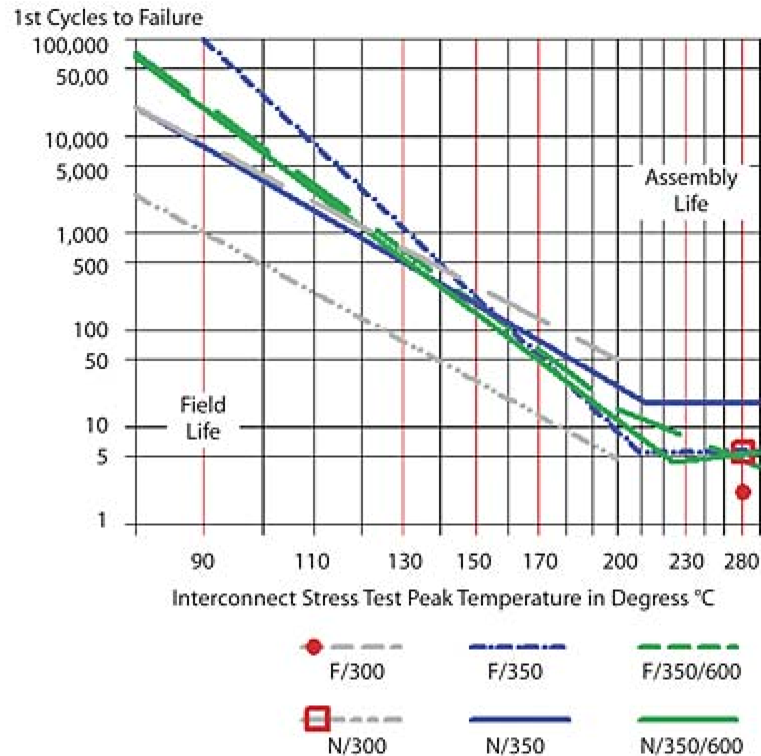
Graph 3. Log-Log plot of life versus stress analysis using the inverse power law.

Graph 3 is obtained from an analysis that used ReliaSoft's ALTA Version 6 and the IST testing at various temperature performed on non-filled vias having a 350micron drilled hole size. Data from testing at 108°C delta (130°C peak) and 128°C delta (150°C peak) is utilized to obtain the IPL coefficients that allow prediction of cycles to failure at a field life peak temperature of 85°C (63°C delta to ambient). A similar graph can be developed for the IST testing at 208°C delta (230°C peak) and 138°C delta (260°C peak) but, due to changes in laminate material properties above Tg, it makes no sense to use the data obtained at 230°C and 260°C to predict field life. The data collected at a 170°C peak temperature was not used because it falls within the Tg transition zone from glass to plastic state where the coefficient of thermal expansion increased 5-6x and storage modulus decreased 18-27x.



Graph 4. IPL plots of temperature stress versus CTF for the non-filled, 350um drilled hole size above and below laminate material Tg. The two sided 90% confidence interval is included with both IPL plots.

Graph 4 shows the combined IPL plots using data from ALTA including CTF below and above Tg. These plots are rather conservative in that they use the lower two sided 90% confidence interval. With the small sample size used, typical six samples per cell, the confidence interval is quite large. Nonetheless, the strong temperature stress versus CTF relationship is clearly seen below Tg. Between 230°C and 260°C the relationship is less clear.



Graph 5. IPL plot temperature stress versus CTF for the two smallest drilled hole size IST designs in the DOE.

The Graph 5 plots do not include the confidence interval for clarity. It clearly shows the difference in slope for CTF versus temperature below and above the laminate material Tg. It is interesting to note that the slope is lower above Tg than it is below Tg. It is felt that this is due to the large decrease in the laminate materials modulus above Tg.

Conclusions

1. IST test to failure at multiple temperatures followed by Lognormal/IPL analysis method provides improved insight into via life versus temperature.

2. The lead-free assembly temperature stress on thick PCB fabs vias that use epoxy/glass laminate materials leaves little margin for error during assembly processing.

3. Rework, if allowed, will need to be carefully controlled.

4. Test to failure at two temperatures above Tg allows prediction of CTF at other temperatures that may be used for lead-free assembly.

5. The filled via process can result in new failure modes and introduces a processing sequence that can adversely affect the reliability of non filled holes when both filled and non filled holes are combined on the same PCB fab panel.

6. There was a low level of failure due to POST interconnect separation (8 of the 278 IST coupons tested) but, the majority occurred at a lead-free peak temperature of 260°C (7 of the 8 at 260°C). This failure mode is rarely seen on high aspect ratios vias at lower temperature and needs to be watched carefully in future IST testing.

Future Work

There are plans to extend the work presented here in the following areas:

- Testing using multiple preconditioning levels at assembly peak temperatures followed by CTF at a temperature below Tg. This data will be used to determine if cumulative fatigue can be estimated using Miner's Rule.

- Investigate the use of alternate test methods like the "Highly Accelerated Thermal Shock" (HATS) in the low temperature region to see if we can get a wider temperature spread than the 108°C to 128°C delta temperatures used here with a goal to get more accurate field life predictions.

- Test at a number of temperatures above Tg to better understand the shape of the CTF curve in this region were it is suspected that new failure modes could dominate (like POST interconnect failures) and result in a Log-Log plot that is not linear.

- Continue to work with Sun's PCB fabrication suppliers and the laminate supplies to develop more robust PCB fabrication process and to qualify epoxy/glass laminate materials suitable for thick PCB fabs and lead-free assembly.

Acknowledgements

This work was supported by Sun Microsystems' Engineering Technologies Group and Scalable Systems Group, PWB Interconnect Solutions, Inc., the University of Maryland/CALCE, and Sun's high-end PWB suppliers, Multek, Sanmina-SCI, and Viasystems.

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