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Deborah Boger, Bill Birch and Susan Mansilla

Abstract

The purpose of this study was to evaluate the performance of technologies that make printed wiring board (PWB) through-holes conductive. Many of these technologies are known as "direct metallization" (DM) processes. In order to complete this evaluation, PWB panels, designed to represent industry "middle-of-the-road" technology, were manufactured at one facility, run through individual "making holes conductive" (MHC) lines at 26 facilities, then electroplated at one facility. The panels were electrically prescreened, followed by electrical stress testing and mechanical testing, in order to distinguish variability in the performance of the MHC Interconnect. The test methods used to evaluate performance were intended to indicate characteristics of a technology's performance, not to define parameters of performance or to substitute for thorough on-site testing; the study was intended to be a "snapshot" of the technologies. This study was carried out as part of the U.S. EPA-Institute for Interconnecting and Packaging Electronic Circuits (IPC) Design for the Environment (DfE) PWB Project and was conducted with extensive input and participation from PWB manufacturers, their suppliers, and PWB testing laboratories. The technologies tested include electroless copper, carbon, graphite, palladium, non-formaldehyde electroless, conductive polymer, and conductive ink. The results of the study suggest that DM technologies perform at least as well as electroless copper if operated according to specifications.

Introduction

Printed wiring boards (PWBs) are an intrinsic part of many products in the electronics, defense, communication and automotive industries. The traditional manufacture of PWBs requires materials and technologies that raise a number of environmental and human health concerns.

Wet chemical processes specifically, such as those used in PWB fabrication, are a significant source of hazardous waste and consume large amounts of water and energy. One such wet chemical process is the method used by PWB manufacturers to make PWB through-holes conductive prior to electrolytic plating. The technology most commonly used today to accomplish this function is the electroless copper process. This technology typically employs formaldehyde as a copper-reducing agent and requires large amounts of water and energy. There are alternative technologies available to accomplish the "making holes conductive" (MHC) function; most of these technologies eliminate the use of formaldehyde and reduce water and energy use, and generate less waste.

The potential environmental and cost advantages of the alternatives are beginning to become apparent and have generated strong interest on the part of industry. Minimal product performance information is publicly available about these technologies, however. To address this data gap, the Design for the Environment (DfE) PWB Project performed a study to evaluate the performance of seven different MHC technologies. The technologies tested include electroless copper, carbon, graphite, palladium, non-formaldehyde electroless, conductive polymer, and conductive ink.* This information will be combined with an evaluation of the relative human health and environmental risk and cost associated with each technology, included in a document titled Cleaner Technologies Substitutes Assessment (CTSA). The CTSA will allow business decision-makers to evaluate the alternatives in terms of the environment, cost, and performance. The PWB CTSA is scheduled to be completed by early 1997.

*The conductive ink test panels were processed through the MHC process and sent for testing. The supplier of the technology felt that because the test vehicle used was incompatible with the capabilities of the conductive ink technology, the test results were not indicative of the capabilities of the technology. Therefore, the results of the conductive ink technology test are not reported.

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Methods and Materials

Test Vehicle Design:

The test panel measured 24" x 18", laminated to .062", with 8 layers. Test panels were produced from B and C stage FR4 materials; detailed artwork is attached as Appendix 1. Appendix 2 shows lamination specifications for the test panels, and a detailed list of the steps taken to manufacture the panels is attached as Appendix 3.

Each test panel contained 54 test coupons: 27 Interconnect Stress Test (IST) coupons (used for electrical testing) & 27 Microsection coupons. IST coupons measure 6.5" x 3/4" and contains 700 interconnecting vias on a 7 row by 100 via 0.050" grid. This coupon contains two independent circuits: the Post circuit and the plated through hole (PTH) circuit. The Post circuit contains 200 interconnects, and is used to measure post Interconnect resistance degradation. The PTH circuit contains 500 interconnects, and is used to measure PTH (barrel) Interconnect resistance degradation. IST coupons had either .013" or .018" holes (finished).

The microsection coupon measures 2" x 2" and contains 100 interconnected vias on a 10 row by 10 via 0.100" grid. It has Internal pads at the second and seventh layer and a daisy chain interconnect between the two surfaces of the coupon through the via. Microsection coupons had either 0.013", 0.018" or 0.036" holes (finished).

Panel Processing:

The detailed workplan for this performance demonstration is attached as Appendix 4.

The general plan for the performance demonstration was to collect information about alternative technologies at sites where the technologies were already in use. The facilities that were used as test sites were identified by suppliers of the technologies being tested. The sites Included production facilities, testing facilities (beta sites), and supplier testing facilities.

For the purposes of this evaluation, the MHC process was defined as everything from the desmear step through 0.1 mil of copper flash plating. In order to minimize differences in performance due to processes outside this defined MHC function, the panels used for testing were all manufactured and drilled at one facility. One hundred panels, described above, were produced.

After drilling, three panels were sealed in a plastic bag with desiccant and shipped to each test site (26 sites total) to be processed through the site's MHC line. All bags containing panels remained sealed until the day of processing. The panels were run through the MHC process at each test site.

An on-site observer was present at each site from the point the bags were opened until processing of the test panels was completed. Observers were present to confirm that all processing was completed according to instructions and to record observations. Each test site's process was completed within one day; it took slightly longer than one month to complete all MHC processing.

After the MHC processing, the panels were put into sealed bags with desiccant and shipped to a single facility, where they remained until all the panels were collected. At this facility, the panels were electroplated with 1.0 mil of copper followed by a tin-lead etch resist, etched, stripped of tin-lead, solder mask coated, and finished with hot air solder leveling (HASL). A detailed account of the steps taken in this process is attached as Appendix 5.

After HASL, the microsection coupons were routed out of the panels and sent to Robisan Laboratory Inc. for mechanical testing. The IST coupons were left in panel format. The panels containing the coupons were passed twice through an IR reflow to simulate assembly stress. A detailed protocol describing the IR reflow process is attached as Appendix 6. The panels with the IST coupons were then sent to Digital Equipment of Canada (DEC) for electrical prescreening and electrical testing.

Electrical Testing:

The IST coupons in panel format were electrically prescreened to determine defects on arrival. The panels were then shipped to another facility for routing of the IST coupons, and which were then shipped back to DEC. Canada for completion of electrical testing.

Electrical testing was completed using the IST technology. IST is an accelerated stress test method used for evaluating the failure modes of printed wiring board interconnect; it uses DC current to create the required temperatures within the interconnect.

There are three principal types of information generated from the IST: initial resistance variability, cycles to failure (barrel integrity), and post separation/ degradation (post interconnect).

Electrical prescreening, used to determine initial resistance variability, was completed on the two circuits in the IST coupons. The resistance value for the first internal circuit (PTH circuit) for each coupon was determined; it gives an indication of the resistance variability (plating thickness) between coupons and between panels. The initial resistance testing was also used to determine which coupons had defects on arrival, or were unsuitable for further testing.

The cycles to failure indicate how much stress the individual coupons can withstand before failing to function (measuring barrel integrity). IST coupons contain a second internal circuit (post circuit) used to monitor the resistance degradation of the post interconnect.

The level of electrical degradation in conjunction with the number of cycles completed is used to determine the presence and level of post separation. The relative performance of the internal circuits indicates which of the two internal circuits, the Post circuit or the PTH circuit, has the dominant failure mechanism. The draft IPC IST test method is attached as Appendix 7.

Mechanical Testing:

The coupons for mechanical testing were sent to Robisan Laboratory Inc. for testing. Mechanical testing consisted of evaluations of metallurgical microsections of plated through holes in the as produced condition and after thermal stress. One test coupon of each hole size from each panel was sectioned. The direction the coupons were microsectioned was determined by visually examining the coupons to determine the direction of best registration to produce the most inner layer circuitry connections in the microsections.

Microsections were stressed per IPC-TM-650, method 2.6.8, attached as Appendix 8. The plated through holes were evaluated for compliance to the requirements found in IPC-RB-276. Microsections were examined after final polish, prior to metallurgical microetch and after microetch.

Selection of Coupons for Testing:

The original test plan called for selection of IST and microsectioning coupons from similar locations on each panel. Following prescreening, the coupon selection criteria was amended to be based on coupons with the best registration. This resulted in some coupons being selected from areas with known thicker copper (see Results of Electrical Prescreening).

Four .013" IST coupons were selected from each of the 3 test panels from each test site. Test sites 3 and 4 had six coupons selected from the two available panels. Three coupons from within six inches of the IST coupons selected were microsectioned from the same panels. In some cases, the desired microsection coupons exhibited misregistration, so next-best locations were used. In all cases, coupons selected were located as close to the center of the panel as possible.

Results:

This performance demonstration was designed as a snapshot. Because the test sites were not chosen randomly, the sample may not be representative of all PWB manufacturing facilities in the U.S. (although there is no specific reason to believe that they are not representative). In addition, the number of test sites for each metallization type ranged from ten to one. Due to the smaller number of test sites for some metallization,

results for these metallizations could more easily be due to chance than the results from metallizations with more test sites. Statistical relevance cannot be determined.

Results of Electrical Prescreening:

Seventy-four of 75 test panels from 25 test facilities were returned. One of the 74 proved to be untestable due to missing inner layers. The results of the prescreening will be reported in the following categories:

1. Defects on arrival (unacceptable for testing)
2. Print and etch variability
3. Plating (thickness) variability

Defects on Arrival:

A total of 1971 coupons from the 73 panels each received two resistance measurements using a 4 wire resistance meter. The total number of holes tested was 1.4 million. One percent (19) of coupons were found to be defective, and were considered unacceptable for IST testing because of opens and shorts.

Defective Coupons Found at Prescreening

Test site #	Metallization	Opens	Shorts
1	Electroless		4
3	Electroless	1	2
11	Graphite	2	
12	Graphite		5
14	Palladium	1	
16	Palladium	2	
20	Palladium	2	

Following an inspection of the defective coupons, the opens were found to be caused by voiding, usually within a single via. Shorts were caused by misregistration. The type of metallization did not contribute to the shorts.

Print Etched Variability:

Throughout manufacturing, the layers/panels were processed in the same orientation, which permitted an opportunity to measure resistance distributions for each coupon/panel. The resistance distribution for the Post circuit was determined. The distribution proved very consistent. This result confirms that inner layer printing and etching did not contribute to overall resistance variability. The table below depicts the mean Post circuit resistance for 5 .013" coupon locations (in milliohms) for all 73 panels.

Mean Post Circuit Resistance Measurements
(Coupon Locations on Panel)

409		405
	399	
415		411

Plating Variability:

The resistance distribution for the PTH circuit was determined; this distribution indicated variability. This result indicated that overall resistance variability was due to plating thickness variability rather than print and etch variability. The tables below depicts the mean PTH circuit resistance for 5 .013" coupon locations (in milliohms) for all 73 panels.

Mean PTH Circuit Resistance Measurements
(Coupon Locations on Panel)

254		239
	244	
241		225

The PTH interconnect resistance distribution showed the electrolytic copper plating increased in thickness from the top to the bottom of each panel. Copper thickness variability was calculated to be .0003" thicker at the bottom compared to the top of each panel. Resistance variability was also found from right to left on the panels; inconsistent drill registration or outer layer etching was thought to be the most probable cause of this variability. (When a number of holes break out of their pads, it increases the internal copper area, causing the resistance to decrease. This reduction in resistance creates the impression the coupons have thicker copper.)

The table below describes the means and standard deviation of all PTH resistance measurements and the levels of correlation between panels observed at each site.

Prescreening Results - .013" Vias for All Test Sites

Site #	Mean Res.	Std Dev.	Pnl #1	Pnl #2	Pnl #3	Corr.
1	239	14.5	234	245	237	ALL
2	252	17.6	269	251	234	2
3	238	12.5	227	248	N/A	ALL
4	232	11.2	224	239	N/A	ALL
5	236	12.1	239	241	229	2
6	266	15.7	255	275	266	2
7	253	14.2	240	259	259	ALL
8	230	11.6	221	228	241	2
9	243	10.6	247	247	235	2
10	248	13.0	256	242	247	ALL
11	226	19.0	216	221	241	2
12	240	23.0	254	235	231	None
13	231	16.0	243	235	215	2
14	247	26.8	256	227	258	ALL
15	243	11.1	236	244	248	2
16	239	15.9	232	243	241	ALL
17	240	12.8	247	243	231	ALL
18	245	9.7	245	249	240	ALL
19	226	10.2	223	232	223	2
20	229	10.2	219	238	229	2
21	250	13.3	258	243	249	2
22	256	8.8	256	261	250	ALL
23	253	12.5	257	257	244	ALL
24	239	12.0	241	232	246	ALL
25	224	13.9	210	232	231	ALL

Note: Only 1 site (#12) was calculated to have poor correlation between all 3 panels. The sample size for each test site = 12

Mean Res = Mean resistance of all coupons (on the three panels)
Std Dev = Standard deviation for all coupons per test site
Pnl # = Mean resistance for listed panel
Corr = Correlation Coefficient >.7 between each panel

As seen in the table above, copper plating distribution at each site was good.

Plating cells and rack/panel locations did not create large variability's that could affect the results of each test site.

Because resistance (plating thickness) distribution was also consistent between test sites (Std. Dev. for mean resistance 10.6 for all test sites), relative comparisons between metallization sites can be made.

It was determined during correlation that the variations in hole wall plating thickness indicated by electrical prescreening was due to variations in the flash plate provided by each test site and not due to variations in electrolytic plating. Remaining test results will be reported by type of metallization. Each metallization type was represented by the following test sites:

Test Site #	Metallization	# of Test Sites
1 - 7	Electroless Cu	7
8 - 9	Carbon	2
10 - 12	Graphite	3
13 - 22	Palladium	10
23 - 24	Non-Formaldehyde	2
25	Conductive Polymer	1

Results of Microsection Evaluation:

The only defects reported in this study were voids in hole wall copper, drill smear, resin recession, and inner layer separation. Average hole wall thickness was also reported for each panel. Defects present, but not included as part of this report are registration, inner layer foil cracks and cracks in flash plating at the knees of the holes. These defects were not included because they were not believed to be a function of the metallization technology. The inner layer foil cracks appear to be the result of the drilling operation and not a result of z-axis expansion or defective foil. None of the cracks in the flash plating extended into the electrolytic plate in the as received coupons or after thermal stress. Therefore, the integrity of the hole wall was not affected by these small cracks.

Plating Voids: There were no plating voids noted on any of the coupons evaluated. The electrolytic copper plating was continuous and very even with no indication of any voids.

Drill Smear: The panels exhibited significant amounts of nailheading. Since nailheading was present on all panels, it was determined that all test sites had received similar panels to process; therefore, comparison were possible. The main concern with the presence of nailheading, was that the amount of drill smear might be excessive compared to each test site's "normal" product. Drill smear negatively impacts inner layer connections to the plated hole wall if not removed.

Resin Recession: No samples failed current specification requirements for resin recession. There was however, a significant difference in the amount of resin recession between test sites. The table below depicts the results of the resin recession evaluation.

Inner Layer Separation: Different chemistries had different appearances after metallurgical microetch. Electroless copper microsections traditionally have a definite line of demarcation between foil copper and electrolytic copper after metallurgical microetch. This line also appeared in electroless copper samples in this study. This line is the width of the Electroless deposit; it is very important in making a determination as to whether inner layers are separated from the plated hole wall.

Many of the products tested in this study had no line of demarcation or lines which had little, if any, measurable width. For those direct metallization products that should not have a line after microetch, the determination as to whether inner layer separation was present on the samples from this study, was based on the presence of a line.

Over half of the test sites supplied product which did not exhibit inner layer separations on as received or thermal stressed microsections. Some of the test sites exhibited product which exhibited inner layer separation in the as received samples and then further degraded after thermal stress. Other test sites had product that showed very good interconnect as received and became separated as a result of thermal stress.

The separations ranged from complete, very wide separations to very fine lines which did not extend across the complete inner layer connection. No attempt was made to track these degrees of separation because current specification requirements dictate that any separation is grounds for rejection of the product.

The following table gives the percentage of panels from a test site that did or did not exhibit a detects. The data is not presented by hole size because only test site 11 had defects on only one size of hole. In all other test sites exhibiting defects, the defects were noted on all sizes of holes.

Test Site #	Percentage of Panels Exhibiting Defect			Panels Exhibiting Defect (avg. Of all test sites)		
	Drill Smr	Res Rec	Post Sep	Drill Smr	Res Rec	Post Sep
1	0	33	0	21	31.6	31.6
2	66	66	100			
3	0	0	0			
4	100	0	0			
5	0	0	0			
6	0	0	100			
7	0	100	0			
8	0	0	0	0	0	0
9	0	0	0			
10	0	0	0	0	11	55.6
11	0	33	66			
12	0	0	100			
13	0	33	0	3.3	26.5	43.3
14	0	0	0			
15	0	0	33			
16	0	0	100			
17	33	33	33			
18	0	33	66			
19	0	100	0			
20	0	0	100			
21	0	0	100			
22	0	66	0			
23	0	0	100	0	0	50
24	0	0	0			
25	0	0	0	0	0	0

The table below depicts the average measured copper plating thickness for all panels.

Microsection Copper Plating Thickness (in Mils)

Test Site	Panel # 1	Panel # 2	Panel # 3	Average Cu
1	1.4	1.1	1.2	1.24
2	0.95	1.1	1.3	1.11
3	1.3	1.1	N/A	1.2
4	1.3	1.2	N/A	1.25
5	1.2	1.3	1.3	1.24
6	1.1	1.1	1.1	1.1
7	1.5	1.1	1.1	1.2
8	1.3	1.3	1.2	1.3
9	1.2	1.4	1.3	1.3
10	1.0	1.1	1.3	1.14
11	1.5	1.5	1.1	1.4
12	1.3	1.3	1.3	1.3
13	1.2	1.3	1.3	1.3
14	1.2	1.1	1.2	1.2
15	1.1	1.1	1.2	1.13
16	1.1	1.2	1.3	1.2
17	1.2	1.3	1.4	1.3
18	1.1	N/A	1.5	1.3
19	1.5	1.3	1.3	1.4
20	1.6	1.4	1.3	1.4
21	1.1	1.2	1.2	1.14
22	1.2	1.1	1.1	1.13
23	1.4	1.1	1.2	1.24
24	1.3	1.2	1.2	1.23
25	1.4	1.7	1.4	1.5

Results of Interconnect Stress Testing:

Test results will be reported in various formats: Both tables and graphs will be used to describe IST cycles to failure for the PTH interconnect and Post degradation/ separation within the Post interconnect. IST was completed on a total of 12 coupons from each test site. The mean cycles to failure for the PTH interconnect are established at the point when the coupon exceeds a 10% increase in the initial elevated resistance.

Mean IST cycles to failure and standard deviation by test site are as follows. (Sample size = 12 coupons from each site):

Test Site # & Metallization Type	IST Cycles to Fail	Standard Dev'n.
1 Electroless	346	91.5
2 "	338	77.8
3 "	323	104.8
4 "	384	70.0
5 "	314	50.0
6 "	246	107.0
7 "	334	93.4
8 Carbon	344	62.5
9 "	362	80.3
10 Graphite	317	80.0
11 "	416	73.4
12 "	313	63.0
13 Palladium	439	55.2
14 "	284	62.8
15 "	337	75.3
16 "	171	145.7
17 "	370	122.9
18 "	224	59.7
19 "	467	38.4
20 "	443	52.5
21 "	267	40.5
22 "	232	86.6
23 Non-Formaldehyde	214	133.3
24 " "	261	41.6
25 Conductive Polymer	289	63.1

The mean IST cycles to failure and standard deviations by metallization technology are as follows:

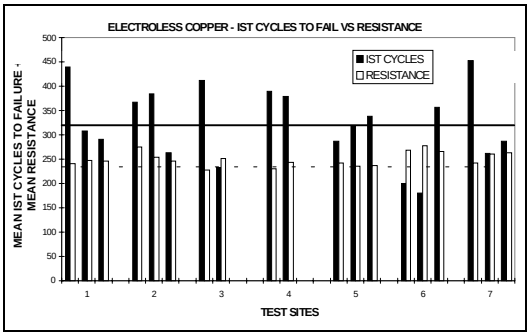
Metallization Technology	IST Cycles to Fail	Standard Dev'n.
Electroless Cu	327	92.5
Carbon	354	71.0
Graphite	349	85.3
Palladium	332	126.0
Non-Formaldehyde	238	99.5
Conductive Polymer	289	63.1

High standard deviations identified that high levels of performance variability exist within and between specific test sites.

The following graphs identify the IST cycles to failure for each panel and test site. The two reference lines on each graph identify the mean cycles to failure (solid line) for all 300 coupons tested (324 cycles) and the mean resistance (dotted line) for all coupons measured (241 milliohms).

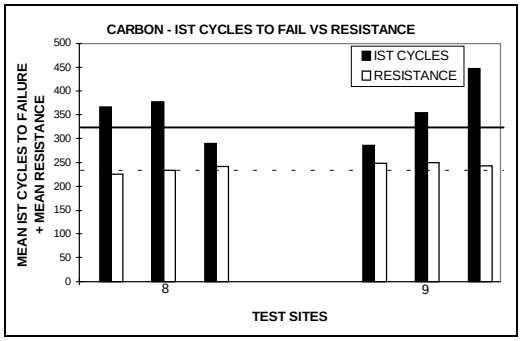
When considering the overall performance of each panel, it is useful to compare the mean resistance of the coupons to the dotted reference line. As mentioned before, each test site was instructed to flash plate .0001" of electrolytic copper into the holes. If the sites exceeded this thickness, the total copper thickness would be thicker, lowering the resistance and increasing the performance of the panels. Therefore, panels with lower resistance should be expected to perform better, and visa versa. Although each site was requested to plate .0001" of electrolytic copper, the actual range was between .00005" and .0005".

The IST cycles to failure for all panels, test sites and metallization technologies are depicted in the graphs below:

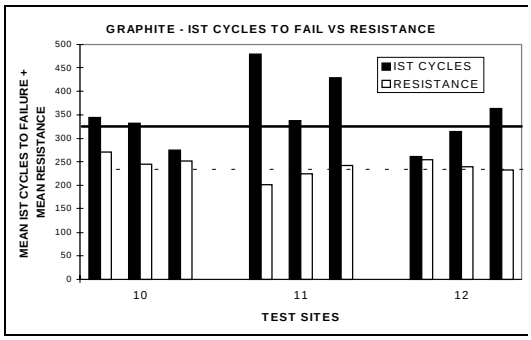


All electroless copper test sites had at least 1 panel that met or exceeded the mean performance. For the panels that did not achieve the mean performance, it can be seen that the mean resistance column was above the reference line (thinner copper). The exception was test site #6, which exhibited a high degree of post

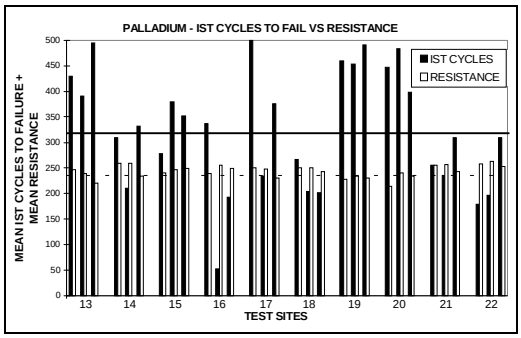
separation (see post separation testing results section for an explanation of results).



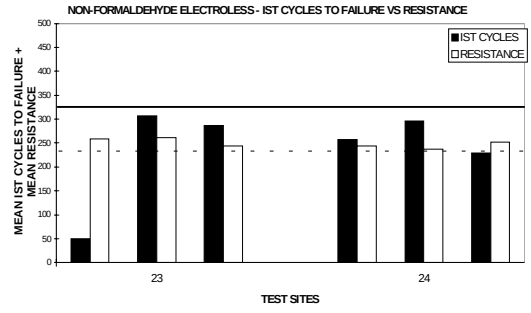
Both carbon test sites had at least 2 panels that met of exceeded the mean performance.



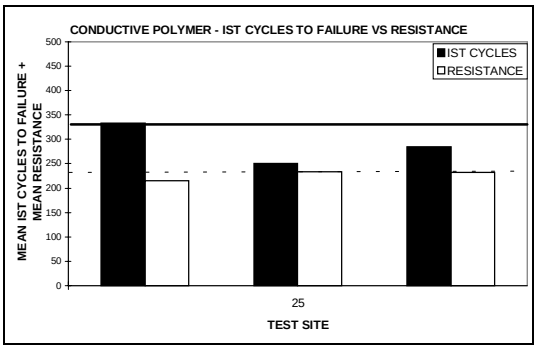
All three graphite test sites had at least 1 panel that met or exceeded mean performance.



Most palladium test sites had at least 1 panel that met or exceeded the mean performance. Three test sites did not. Those test sites that did not achieve the mean performance exhibited either high resistance or post separation.



Neither non-formaldehyde electroless copper test site met or exceeded mean performance. Test site 23 exhibited a high degree of post separation (see post separation results section for an explanation of results).



The single conductive polymer test site had one panel that met or exceeded the mean performance.

Post Separation Testing Results:

IST determines post interconnect performance (post separation) simultaneously with the PTH cycles to failure performance. The failure criteria for post separation has not been established. Further work is in progress with the IPC to create an accept/reject criteria.

For this study, the IST rejection criteria is based on a 15 milliohm resistance increase derived from the mean resistance degradation measurement for all 300 coupons tested.

A reliable post interconnect should measure minimal resistance degradation throughout the entire IST. Low degrees of degradation (<15 milliohms) are common and relate to the fatigue of the internal copper foils. Resistance increases greater than 50 milliohms were reported as 50 milliohms. This was done in order to avoid skewing results.

The mean resistance degradation of the post interconnect is determined at the time the PTH failed. The readings (in milliohms) for the Post interconnect and the standard deviations for each test site were as follows (sample size = 12 coupons from each site):

Test Site # and Metallization type		Post Degrad'n.	Standard Dev'n.
1	Electroless	13.1	3.5
2	"	17.2	12.9
3	"	6.6	3.7
4	"	6.7	2.7
5	"	3.8	2.4
6	"	34.8	13.1
7	"	4.1	4.6
8	Carbon	2.8	2.9
9	"	2.0	2.5
10	Graphite	5.2	3.9
11	"	8.0	8.1
12	"	16.0	15.0
13	Palladium	9.5	4.7
14	"	2.8	2.6
15	"	7.9	7.4
16	"	32.2	18.1

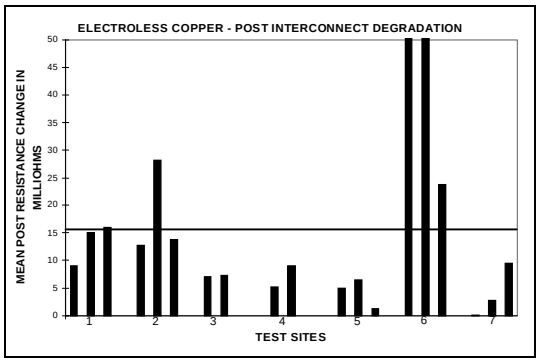
17	"	0.8	1.8
18	"	7.6	6.4
19	"	4.7	3.3
20	"	13.7	5.6
21	"	40.5	11.3
22	"	4.5	2.6
23	Non-Formaldehyde	47.9	7.2
24	" "	4.2	1.9
25	Conductive Polymer	2.8	1.8

The mean Post interconnect resistance degradation (in milliohms) and standard deviations for each metallization technology were as follows:

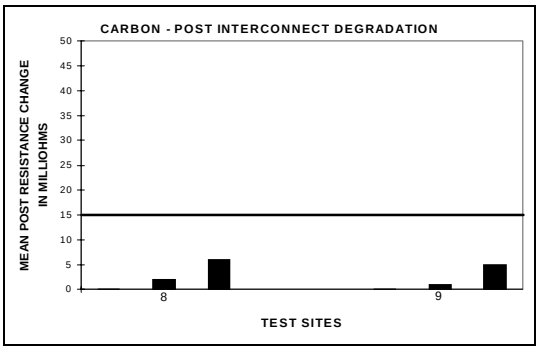
Metallization Type	Post Degrad'n.	Standard Dev'n.
Electroless Cu	12.3	12.6
Carbon	2.4	2.7
Graphite	9.7	10.8
Palladium	12.4	14.3
Non-Formaldehyde	26.0	22.9
Conductive Polymer	2.75	1.8

High standard deviations identified that high levels of variability exist within and between specific test sites and within a metallization technologies.

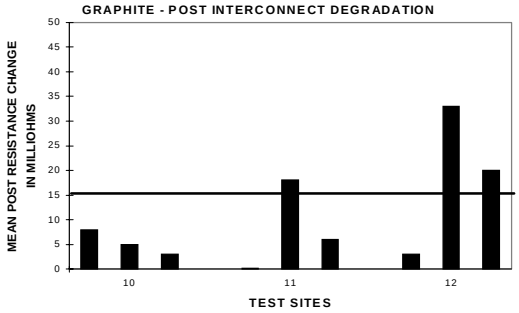
The following graphs identify the mean (average of 4 coupons per panel) IST Post resistance degradation results. The reference line on each graph identifies the mean resistance degradation measurement for all 300 coupons tested (15 milliohms). If the mean resistance degradation column is above the reference line, the panel had coupons that exhibited post separation. The post resistance change was the value recorded at the point where the PTH (barrel) failed.



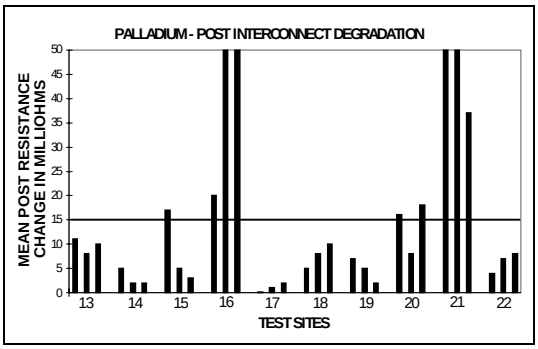
Two of the seven electroless copper test sites had at least 1 panel that exhibited post separation. All 3 panels in test site 6, clearly exhibited gross post separation.



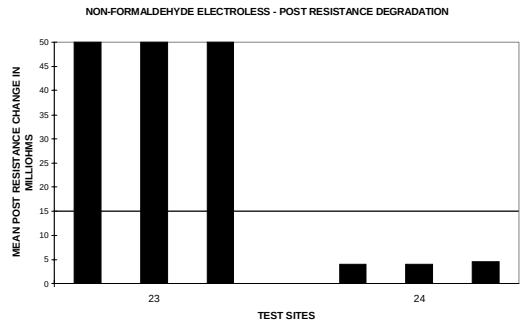
No post separation was detected on any carbon panels.



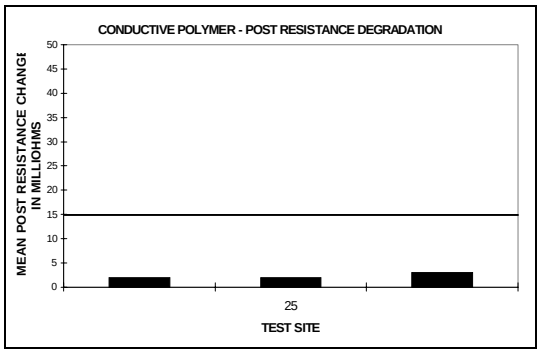
Two of the three graphite test sites had at least 1 panel that exhibited post separation.



Four of the ten palladium test sites had at least 1 panel that exhibited post separation. Test sites 16 and 21 clearly exhibited gross post separation.



All 3 panels for non-formaldehyde electroless copper test site 23 clearly exhibited gross post separation.



No post separation was detected on any conductive polymer panels.

Comparison of Microsection and IST Test Results:

Microsection and IST were run independently, and test results were not shared until both sets of data were completed and delivered to EPA.. To illustrate the consistency of the test results, the table below identifies both test methods and their results for post separation detection.

IST/Microsection Data Correlation

Test Site #	Micro-section	Panels affected	IST	Panels affected
1	N	0	N	0
2	Y	3	Y	3
3	N	0	N	0
4	N	0	N	0
5	N	0	N	0
6	Y	3	Y	3
7	N	0	N	0
8	N	0	N	0
9	N	0	N	0
10	N	0	N	0
11	Y	2	Y	1
12	Y	3	Y	2
13	N	0	N	0
14	N	0	N	0
15	Y	1	Y	1
16	Y	3	Y	3
17	Y	1	N	0
18	Y	2	Y	2
19	N	0	N	0
20	Y	3	Y	2
21	Y	3	Y	3
22	N	0	N	0
23	Y	3	Y	3
24	N	0	N	0
25	N	0	N	0

Note: Y or N (yes or no) denote whether post separation was detected on any coupon or panel from each test site. The “panels affected” column refers to how many of the panels within each test site exhibited post separation.

Test site 17 was the only site that post separation was found in the microsection but not on IST.

Discussion:

This study was a snapshot based on products built with B and C stage FR4 materials and this specific board construction. The data can not necessarily be extrapolated to other board materials or constructions.

Product performance for this study was divided into two functions: PTH cycles to failure and the integrity of the bond between the internal lands (post) and the PTH. The PTH cycles to failure observed in this study is a function of both electrolytic plating and MHC process; the results indicate that each MHC technology has the capability to achieve comparable (or superior) levels of performance to electroless copper.

Post separation results indicated percentages of post separation that were unexpected by many members of the industry. It was apparent that all MHC technologies, including electroless copper, are susceptible to this type of failure.

The results of this study further suggest that post separation may occur in different degrees. The level of post separation may play a role in determining product performance; however, the determination of levels of post separation remain to be discussed and confirmed by the PWB industry.

Site number 6, an electroless copper site, may not have performed to its true capability on the day of the test. Due to a malfunction in the line, the electroless copper baths was controlled by manual lab analysis instead of by the usual single-channel controller. Both test methods failed all panels from test site 6 for post separation.

Fine line evaluations in microsections have always been a point of contention within the industry. Current microsection specifications state that any indication of separation between the hole wall plating and the inner layer is sufficient grounds to reject the product. An indication of post separation would be a black line on the microsection thicker than what normally appears with electroless copper technology (normal avg: 0.02-0.04mils).

Separation may also be determined by a variation in the thickness of the line across the inner layer connection, especially on electroless deposits that are very thin. The rationale for these rejection criteria is that product with post separation degrades with time and temperature cycling.

With traditional electroless copper products where post separation is present, it can usually be determined where the separation occurs: between the electroless and foil, within the electroless or between the electroless and the electrolytic plating. This determination often helps in troubleshooting the plating process.

In this study, some of the direct metallizations resulted in no line at all after microetch on the microsections. This posed a problem in interpretation of results.

If traditional criteria is used to determine inner layer separation (i.e. the line of demarcation is thicker on some inner connects than others, and the electroless can be seen as continuous between the inner layer and plated copper), then accurate evaluations of product with no lines would not be possible. In this study, the criteria used on “no line” products was that if the sections exhibited any line of demarcation after microetch, the product is considered to have inner layer separation.

This issue is significant to the PWB industry because there remains a question about the relationship

between the appearance of a line on the microsection to the performance of a board.

Traditionally (with electroless copper products), the appearance of a line thicker than normal electroless line is considered to be post separation, and the board is scrapped. However, there are no criteria for how to evaluate "no line" products. In addition, there are no official means of determining when "a little separation" is significant to the performance of the board.

IST is not a subjective test and is not dependent upon the presence or absence of a line in a microsection after microetch. The test provides a relative number of IST cycles necessary to cause a significant rise in resistance in the post interconnect. This number of cycles may be used to predict interconnect performance. Tests such as this, when correlated with microsections, can be useful in determining how to interpret "no line" product characteristics. In addition, IST may be able to determine levels of post separation.

The figures included in Appendix 7 show various failure mechanisms exhibited by different test sites and panels. Future industry studies must determine the relevance of these curves to performance, based on number of cycles needed to raise the resistance as well as the amount of change in resistance. Definitions for "marginal" and "gross" separations may be tied to life cycle testing and subsequently related to class of boards produced.

Acknowledgments

The authors of this paper would like to thank all project participants for their outstanding level of commitment and participation in support of this project. Participants in the performance demonstration have been particularly involved in lending technical expertise and direction for a successful evaluation of the technologies. Suppliers that have submitted technologies for evaluation in the performance demonstration include Atotech USA; Electrochemicals Inc.; Enthone-OMI Inc.; LeaRonal Inc.; MacDermid Inc.; Shipley Co.; Solution Technology Systems; and W.R. Grace & Co.

In addition, a number of companies have volunteered their time and resources to take part in completing the performance demonstration. H-R Industries Inc., manufactured and drilled the panels using laminate donated by ADI/Isola. Once they had been processed through the individual sites' MHC lines, Hadco Corp. processed the panels with dry film donated by Dupont Corp. Hadco Corp. electroplated the panels, routed the microsection coupons, and performed an IR reflow on the IST coupons.

DEC Canada volunteered its resources for IST electrical stress testing, Robisan Laboratory volunteered to do the mechanical testing of the coupons at a drastically reduced cost. Circo Craft volunteered its resources to complete Scanning Electron Microscopy and statistical analysis. The performance testing occurred in 26 sites, domestic and international, and the DfE PWB Project would especially like to thank those sites for volunteering their time and labor to successfully complete this study.

In addition, the authors would like to thank Gary Roper, H-R Industries Inc., for serving as co-chair of the Performance Demonstration workgroup, and Kathy Hart, U.S. EPA, and the rest of the DfE PWB Project Core Group for its support of the performance testing. We would also like to thank the IPC Electroless/Electrolytic Task Group for keeping close track of our work and allowing us generous time on its agendas.

Appendices:

1. Test panel artwork
2. Test panel lamination specifications
3. Panel manufacturing: step-by-step list
4. Performance demonstration workplan
5. Panel plating etc.: step-by-step list
6. IR reflow protocol
7. Draft IPC IST Test Method
8. IST data analysis
9. RB-276 protocol

Appendix 2: Lamination Specifications for DfE Performance Demonstration Panels

Layer	Core	Item Description	Copper oz	Material Thickness	Qty Per.
1		Copper Foil 0.5		0.0007	1
		Prepreg 1080		0.0026	2
2/3	1	Standard Core .006	1/1	0.0060	1
		Prepreg 7628		0.0066	2
4/5	2	Standard Core .006	1/1	0.0060	1
		Prepreg 7628		0.0066	2
6/7	3	Standard Core .006	1/1	0.0060	1
		Prepreg 1080		0.0026	2
8		Copper Foil 0.5		0.0007	1
Total Thickness				0.0562	

Board Type:	8 layer multilayer
Board Technology:	Through-hole
Board Dimensions:	15.587 x 20.758
Material Grade:	FR-4
Panel Size:	18” x 24”
Line width:	0.0200
Spacing:	0.0140
Overall Calculated Press Thickness:	0.062 +/- 0.009

Appendix 3: Process Steps for Manufacturing and Drilling DfE Performance Demonstration Panels

1. Clean
2. Laminate dry film
3. Over layers
4. Image
5. Develop
6. Etch/Strip
7. Optical inspect
8. Mechanical inspect
9. Black oxide
10. Converter
11. Bake @250C for one hour
12. Lay-up/press
13. Final inspection
14. Drill
15. Put panels in bags with desiccant
16. Ship panels to individuals MHC test sites

Appendix 4: Design for the Environment Printed Wiring Board Project Performance Demonstration Workplan

Note: This workplan provides the general protocol for the Design for the Environment (DfE) Printed Wiring Board (PWB) Project Performance Demonstration, which will generate information for the PWB Cleaner Technologies Substitutes Assessment (CTSA) on the "making holes conductive" step of the PWB manufacturing process. The workplan is based on input from representatives of the PWB industry, industry suppliers, EPA, the University of Tennessee Center for Clean Products and Clean Technologies, and other stakeholders of the DfE PWB Project. There may be slight modifications to the workplan as preparations for the performance demonstration progress.

I. OVERVIEW

A. Goals

The overall goal of this performance demonstration is to obtain specific information about alternative technologies that effectively make holes conductive. Specifically, the goals are the following: 1) to encourage PWB manufacturers to experiment with new products and workpractices that may reduce environmental and human health risk and result in pollution prevention; 2) to standardize existing information about commonly used technologies; and 3) to gain information about technologies not in widespread use, emerging technologies, or technologies that may be applicable to making holes conductive.

B. General Performance Demonstration Plan

The general plan for the performance demonstration is to collect information about alternative technologies at sites where the technologies are already being used. These sites may be customer production facilities, customer testing facilities (beta sites), or supplier testing facilities, in that order of preference. The test vehicle will be a standardized 8-layer multilayer board that has been used by industry to evaluate accelerated board testing methods. Every attempt will be made to limit the variability associated with the boards that is not due to differences in the technologies being tested. The boards will be produced specifically for this performance demonstration. Information will be collected from each demonstration site during the testing.

C. Characteristics of Alternative Technologies to be Reported from Performance Testing

1. Product cost: cost per square foot of panel processed

   This number will be based on information provided by product suppliers, such as purchase price, recommended bath life and treatment/disposal methods, and estimated chemical and equipment costs per square foot panel per day. "Real world" information from PWB manufacturers, such as actual dumping frequencies, treatment/disposal methods, and chemical and equipment costs will be included. The product cost may differ for different shop throughput categories.

2. Product constraints: with which types of board shop processes is the product compatible

   This information will be submitted by the manufacturers and may also be identified as a result of the performance testing.

3. Special storage, safety and disposal requirements: Flammability or volatility of the product, VOCs, TTOs, HAPS, Prop. 65 chemicals

   This information will be requested from the manufacturers and will vary according to the chemicals comprising the products. Manufacturers will provide recommendations on disposal or treatment of wastes associated with the use of their products. The storage and disposal costs will be a factor in determining the adjusted cost of the product.

4. Ease of use: physical effort required to effectively use the product line, convenience

   This is a subjective, qualitative measurement based on the judgment of the product user. Specific questions such as the following will be asked: How many hours of training are required to use this product? What process parameters are needed to ensure good performance? What are the ranges of those parameters and is there much flexibility in the process steps?

5. Duration of production cycle: the measured time of the "making holes conductive" process, number of operators

   This information will be used to measure the labor costs associated with the use of the products. Labor costs will be based on the time required for making holes conductive with the specific products and at a standard worker wage. The product cycle has been defined as the desmear step to a flash up to 0.1 mil (includes desmear and flash).

6. Effectiveness of technology, product quality:

   These characteristics will be assessed based on performance standard measurements such as aspect ratio plated, solder float test, thermal cycling, yield, and CpK (process capability).

7. Energy and natural resource data:

   This information will be used to measure energy consumption and the variability of energy consumption for the use of different technologies. Measurements of duty and load, for example, will be collected. The information will also address materials use rates and how the rates vary with alternative processes.

8. Exposure data:

   This data will be used to characterize exposures associated with technologies not in widespread use. Exposure information for more commonly used technologies will be collected in the workplace practices survey, conducted separately from this study.

II. PERFORMANCE DEMONSTRATION PROTOCOL

A. Technologies to be Tested

1. Electroless copper
2. Carbon-based
3. Graphite-based
4. Palladium-based
5. Non-formaldehyde electroless
6. Conductive polymer
7. Conductive inks

B. Step One: Identification of Suppliers and Test Sites/Facilities

Workgroup members will identify any additional suppliers of the above product lines and participate actively in soliciting supplier participation in the performance demonstration. Any supplier that wishes to participate will be eligible to submit their technology, provided that they agree to comply with the testing protocol and submit the requested information.

Suppliers will identify sites that are using their product lines/technologies to make holes conductive according to the priority sites listed below.

First preference for testing sites: customer production facilities
Second preference for testing sites: beta sites - customer testing facilities
Third preference for testing sites: supplier testing facilities

Every vendor is guaranteed testing at one site; a submission of a second site will be subject to the review of the performance demonstration workgroup. The workgroup will decide how many submissions are feasible based on time and resource constraints. If a supplier has more than one substantially different product line, it may submit names of test facilities for each of the product lines.

C. Step Two: Test Vehicle Production and Characteristics

In order to minimize the variables associated with panel production, one manufacturer will produce all of the panels. The time and materials to produce the panels will be donated to the project by industry members. The manufacturer will produce enough 18" x 24" 8-layer multilayer panels to send three panels to each test facility. The artwork and detailed characteristics for the panels are being developed separately in IPC's electroless/electrolytic plating subcommittee. Detailed construction information, when available will be attached to the performance demonstration workplan. The panels will have the following characteristics:

Material: FR 4 Fiberglass Resin
Laminate thickness: .062 inches
Hole sizes: multiple holes of sizes .013, .018, and .036 inches

The boards will be manufactured at a single shop stopping before the desmear step. Three panels will be shipped to each test facility to be run through the making holes conductive line, which begins with the desmear step. A permanganate desmear including an organic sensitizer (pretreatment) will be used on all panels.

D. Step Three: Making Holes Conductive

The panels, once distributed to testing facilities, will be run through the making holes conductive (MHC) process line in operation at the facility. The usual process operator will operate the line in order to minimize error due to unfamiliarity with

the technology. The panels will all be processed in the same production run. In order to ensure compatibility with desmear processes, the panels will be desmeared and run through the MHC line at the individual facilities.

Panels that are manufactured with the pattern plate process will be treated slightly differently than panels manufactured with the panel plate process. Panels manufactured with the pattern plate process will first go through the MHC line. Dry film will be applied, and the panels will be developed to remove all resist. The panels will then be flash plated up to 0.1 mil.

Panels that are panel plated will first go through the MHC line, and then be directly flash plated up to 0.1 mil. This process was designed to ensure that resist residues don't interfere with the through-hole plating process. (Note: the process was not meant to test the adhesion of the resist to the panel or to test resist compatibility with different processes.)

After the holes have been flashed to 0.1 mil of electroplated copper, the individual test facilities will ship all of the panels to a single plating facility where the panels will be electroplated. This procedure will minimize variability due to variation in electroplating techniques.

E. Step Four: Information Collection at Demonstration Facilities

An independent observer will be present when the panels are run through MHC product lines at demonstration facilities. The observer will record information on an Observer Data Collection Sheet during the test. The information requested on this data collection sheet will be discussed with the operator prior to the test.

F. Step Five: Electroplating and Testing of the Boards

After the panels have been completed (holes made conductive and flashed up to 0.1 mil) at the different testing sites, they will be collected at a facility where they will be electroplated to a thickness of 1 mil. Once finished, the boards will be electrically tested using Interconnect Stress Test (IST) methodology. In addition, they will be microsectioned, and tests such as solder shock and thermal cycling will be conducted to ascertain the following characteristics:

1. Aspect ratio effectively plated
2. Solderability
3. Cycling time
4. Ability to cover powder debris
5. Yield
6. CpK (process capability)
7. Coverage, voids, shoulders, modes of failure in shock test

The test protocol is being developed separately in IPC's electroless/electrolytic plating subcommittee. This protocol will be attached to the performance demonstration workplan. Mechanical board testing will be done at an independent laboratory.

III. PERFORMANCE DEMONSTRATION PARTICIPANT REQUIREMENTS

A. From the Facilities/Process Operators:

1. Facility will make their process line/process operators available to run 3 panels in the designated performance demonstration time frame.

2. The process operator will meet with the independent observer briefly before running the first panel through the line to familiarize him/her with the unique aspects of the line. The process operator will be available to assist the independent observer in collecting information about the line when the panels are run through it.

B. From the Vendors/Suppliers of the Process Line Alternatives:

1. Vendors will identify demonstration sites.

2. Vendors will submit product data sheets, on which they will provide information on product constraints, recommended disposal/ treatment, product formulations, etc. The requested information will be agreed upon prior to testing.

Appendix 5: Process Steps for Electroplating, Etching, HASL and IR Reflow of DfE Performance Demonstration Panels

1. Drill to create tooling holes
2. Apply plating resist (organic photopolymer) - image and develop
3. Electroplate copper
4. Apply etch resist (tin)
5. Strip plating resist
6. Etch

7. Strip etch resist
8. Solder mask - image and develop
(Send panels for conductive ink process)
9. Hot air solder leveling (HASL)
10. Rout out AT&T B coupons, place in numbered bags
11. Send AT&T B coupons to Robisan Laboratory Inc.
12. Send panels for IR Reflow
13. IR Reflow
14. Package and ship panels to DEC Canada for electrical testing

Appendix 6: Activities with the I.P.C. and I.S.T. Partners

- Completed repeatability and reproducibility studies with multiple IST users and traditional test labs
- Determine the applicability of the I.S.T. approach to effectively quantify the presence and influence of post separation on PTH interconnect reliability
- Establish impact of various assembly conditions on long term reliability of total interconnect
- Review ongoing performance/development efforts at IPC committee meetings
- IST technology selected as test method to quantify via registration & reliability of Micro-via technologies (ITRI)

Appendix 7: Specifications for IR Reflow of DfE Performance Demonstration panels

The panels containing only IST coupons were processed through a surface mount technology (SMT) oven with the following specifications:

Oven Model	BTU VIP98 Unit
Oven Profile (top and bottom)	Zone 1 = 200 C Zone 2 = 180 C Zone 3 = 170 C Zone 4 = 180 C Zone 5 = 190 C Zone 6 = 240 C Zone 7 = 240 C
Processing Speed	30 inches/minute
Panel Orientation	#1 edge up and leading; shorter (18") edge leading
Panel Spacing	24 inches or 48 seconds
Oven Passes	Two - first 12/29/95 1540 to 1745 second 12/30/95 0801 to 1015
Oven Carrying Support	Wire conveyor
Cooling Between Passes	Horizontally in metal rack, room temperature

*Note: Only IST coupons were processed through IR Reflow

Appendix 8: IPC-TM-650 #2.6.26

This test method manual is available on PWB's webb site under documentation test methods

Appendix 9: IPC TM 650: Protocol for Thermal Stress Test for Plated-Through Holes, Number 2.6.8

1. **Scope**

To standardize the thermal stressing methodology for subsequent evaluation of the copper plating in through holes after exposure to high temperature solder float. The test may be performed on plated-through holes after any stage of plating, i.e., copper, nickel, gold, tin, etc.

2. **Applicable Documents**

Federal specifications QQ-S-571 and MIL-F-14256, and IPC-TM-650. Test Method 2.1.1.

3. **Test Specimen**

3.1 Specimen shall be removed from the panel by sawing or equivalent method, 1/4" from the edge of terminal pad area of through holes to be tested.

3.2 Specimens shall be sawed from a printed wiring board or test coupon in such a manner that at least three of the smallest size plated-through holes can be viewed in the finished microsection.

4. **Apparatus**

4.1 Circulating Air Chamber. Capable of maintaining a uniform temperature of 135 C (275 F) to 149 C (300 F).

4.2 Solder Pot. Electrically heated, thermostatically controlled of sufficient size containing at least 2 pounds of SN63 percent solder conforming to the contaminant level specified in Table II of IPC-S-615.

4.3 Thermocouple indicator. Or other devices to measure the solder temperature 3/4" +/- 1/4" below the surface.

4.4 Desiccator

4.5 Microscope. Range (100x/400x)

4.6 Stop Watch

4.7 Water White Rosin Flux. Type R per MIL-F-14256 or flux agreed upon between customer and vendor.

5. Procedure

5.1 Specimens shall be conditioned by drying in an over for a minimum of 4 hours at 135 C (275 F) to 149 C (300 F) and cooled to room temperature in a desiccator.

5.2 Remove the specimens from the desiccator using tongs. Flux coat the surface and plated-through holes to insure solder slugging.

5.3 Remove the dross from the solder pot surface and lay the specimen on the solder maintained at 288 C (550 F) +/-5 C (+/-9 F) for 10 seconds +1. -0 seconds. (The specimens are not to be held against the surface of the molten solder.)

5.4 Using tongs, carefully remove the specimen from the solder and allow to cool to room temperature.

Caution: Do not shock specimens while the solder in the plated-through hole is still liquid.

5.5 Microsection as defined in Test Method 2.1.1 of IPC-TM-650 and examine plated- through holes for degradation of the plated metal or the foil.