PWB Interconnect Solutions Inc.

Accelerated Stress Testing of the Total Interconnect using I.S.T. Technology

AGENDA

- ***PWB INTERCONNECT/I.S.T. HISTORY***
- ***OVERVIEW OF I.S.T. TEST SERVICE ACTIVITIES***
- ***ALTERNATIVE TEST METHODS***
- ***I.S.T. PRINCIPLES AND METHODOLOGY***
- ***TEST COUPON DESIGN CONSIDERATIONS***
- ***CORRELATION STUDIES***
- ***INTERCONNECT SEPARATION TESTING***
- ***I.S.T. DATA ANALYSIS***
- ***I.P.C. ACTIVITIES***

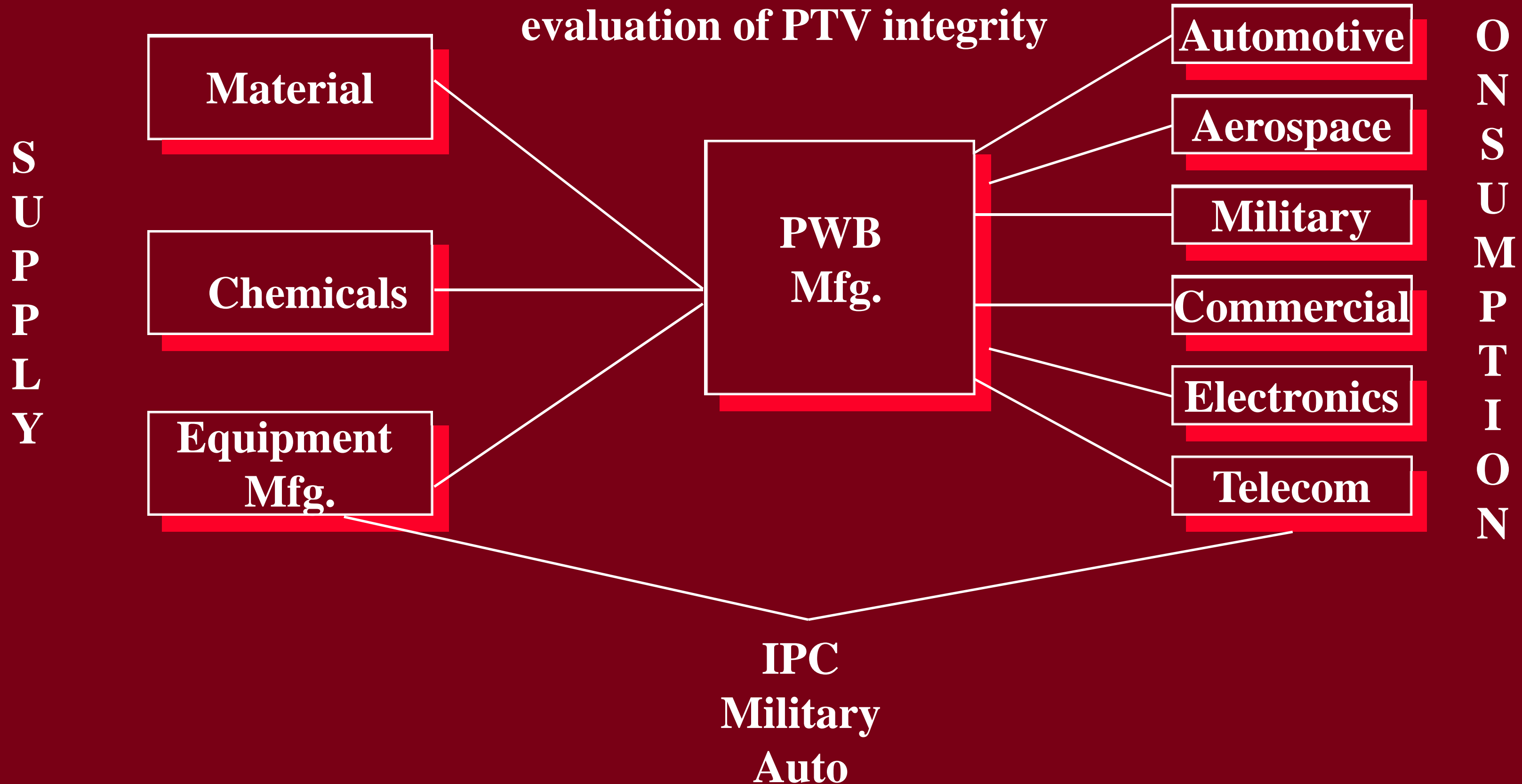
I.S.T. SYSTEM DEVELOPMENT Chronology (8 years)

- *IST Principles developed (1991)*
- *Beta systems deployed (1993)*
- *Patents received (1994)*
- *Interconnect testing introduced (1995)*
- *IST licensed to PWB Interconnect Inc. (1996)*
- *IST Systems delivered to customers (96/97)*
- *IPC approved test methodology (2.6.26) (1997)*
- *Expanded into Europe and Asia (98/00)*

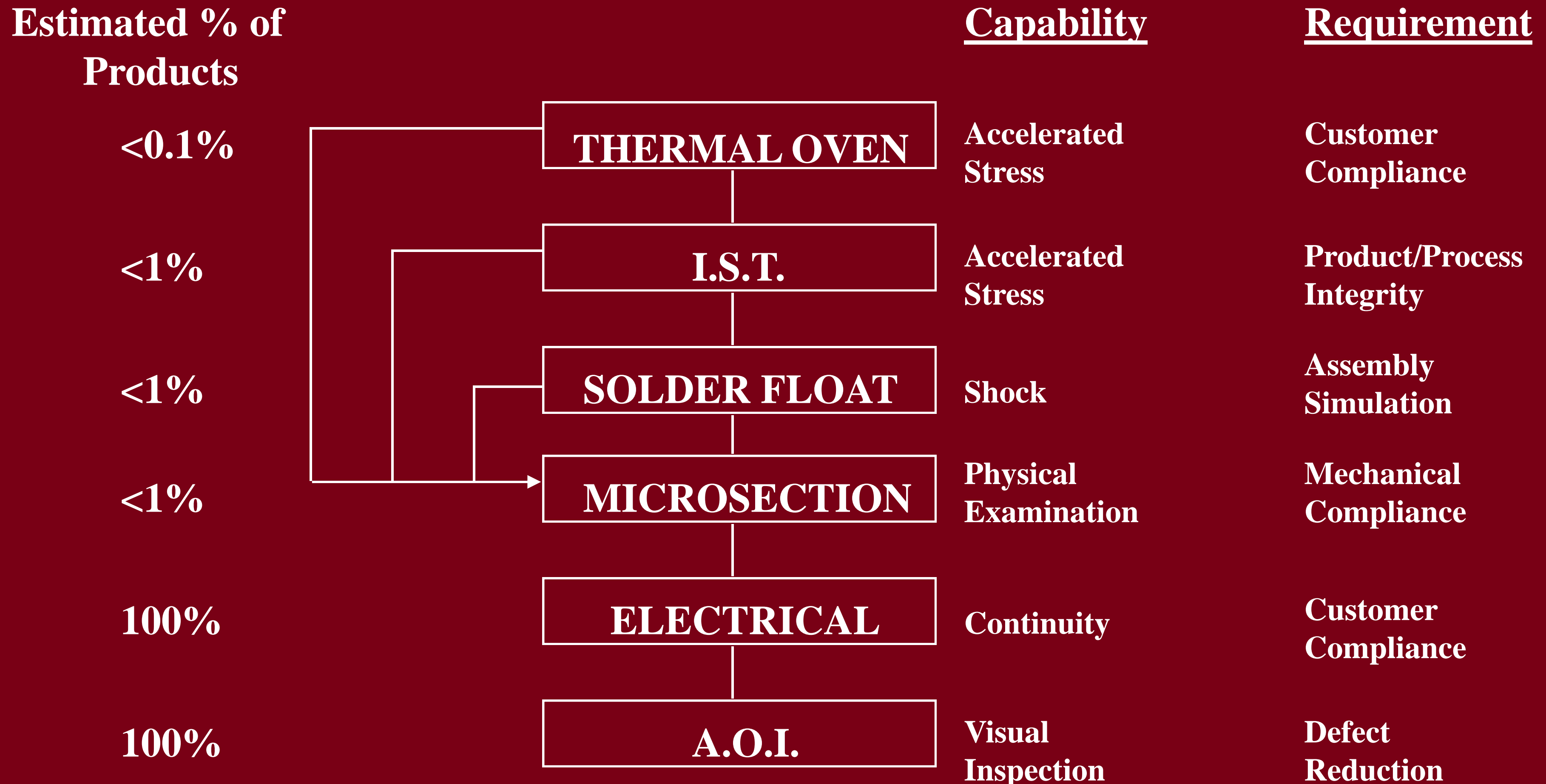
PWB Interconnect Solutions Inc.

- *Owned/Operated by I.S.T. innovators*
- *Exclusive License with Compaq Computers.*
- *Businesses - IST systems / Test services / Consulting*
- *18 system installations in N.A., Europe, Asia*
- *Negotiating additional systems - Worldwide*
- *Eight systems supporting test services, 3 additional systems to be added Q2/00*
- *I.S.T. user group established*
- *Developing new IST system software in Visual, and future capability to test solder joint reliability*
- *Established Support Centers within U.S. & Asia + Independent test service contractors*

I.S.T. STRATEGY



PWB TESTING HIERARCHY



COMPANIES USING I.S.T. TECHNOLOGY/SERVICES

ADVANCED CIRCUITS - ADVANCED QUICK CIRCUITS - ALLIED SIGNAL - ALTRON - AMBITECH - AMP CIRCUITS - ATOTECH AUTOMATA - BLASBERG OMI - BOEING - CELESTICA - CISCO COMPAQ COMPUTERS - COMPEC - DELPHI ELECTRONICS - DELL COMPUTERS - DY4 - DYNAMIC DETAILS - ELEC & ELTEK ELECTROCHEMICALS - GENERAL INSTRUMENTS - GOLD CIRCUITS GRAPHIC RESEARCH - HADCO CORP - HITACHI - HONEYWELL HEWLETT PACKARD - IBM - INTEL - ITRI - JOHNSON MATTHEY KODAK - LOCKHEED MARTIN - MAXEDGE - MERCURY COMPUTERS MERIX CORP - MOTOROLA - MULTEK - NAN YA - NASA - NELCO NORTHERN TELECOM - PARLEX - PARAGON - PC WORLD PHOTOCIRCUITS - PRAEGITZER IND. - RAYTHEON - ROCKWELL COLLINS - SANDERS - SANMINA - SATURN ELEC - SILICON GRAPHICS - SHIPLEY-RONEL - SPECTRIAN - SUN MICROSYSTEMS SYMBOL TECHNOLOGY - TELEDYNE TERADYNE - TOPPAN - TRW TYCO - UNICAP - UNIVERSAL CIRCUITS - VIASYSTEMS - WUS

I.S.T. TECHNOLOGY / SERVICE UTILIZATION

- *Process / Product characterization (Baselining)*
- *Material / Chemical evaluations*
- *Process troubleshooting*
- *PWB vendor base assessment*
- *Impact of assembly/rework stresses*
- *Correlation studies*
- *Customer assurance*
- *Product prescreening for long term testing*
- *Reduction of microsectioning and accelerated stress test levels/costs*

MOST COMMONLY TESTED ATTRIBUTES

Materials	Tetra - Multi FR4's
Hole Sizes	.010" - .024"
PWB Thickness	.062" - .093"
Aspect Ratio	5:1
Via Types	Thru/Blind/Micro
Layers	6-12 Layers
Interconnects	PTH / Post
Metallizations	Electroless/Directs
Plating Thickness	.0005" - .002"
Test Temperatures	150C

CUSTOMER ATTRIBUTES TESTED IN LOWER VOLUMES

■ *Materials*	*Med/High Tg FR4's, Teflon Thermount, Filled/Unfilled*
■ *Hole Sizes*	*.003" Micro-via*
■ *PWB Thickness*	*.100"+ thru .300"+*
■ *Via Types*	*Blind, Buried, Controlled depth, Thermal, Plugged*
■ *Via Construction*	*Drill, Laser, Photochemical, Plasma*
■ *Layers*	*Sequentially Laminated*
■ *Interconnects*	*Via in pad/Microwire*

ATTRIBUTES TESTING UNDER DEVELOPMENT

■ *Metallization*	*Direct Plates*
■ *Finishes*	*HASL/OSP/Au/Sn/NiAu/ Ag/Pd/Bi/CuNiCu*
■ *Plating Thickness*	*.0003” - .004”*
■ *Test Temperatures*	*170C - 200C*
■ *Thermal Isolation*	*Heat-sinking into PWB*
■ *Ongoing concerns*	*Pads Vs No pads* *Plating Variability* *Hole Breakout* *Post Separation/Foil Cracks*

WHY DO WE NEED NEW STRESS TEST METHODS ?

THERMAL OVEN / LIQUID TO LIQUID / SAND BATH / SOLDER FLOAT

- *Industry wide studies over the last ten years have concluded that traditional methods are:*
  - *Too Slow*
  - *Non Repeatable/Reproducible*
  - *Difficult to correlate between methods*
  - *Difficult to characterize and do not simulate the products expected assembly/environmental conditions.*
  - *Too expensive*
  - *Extensive microsectioning required*
  - *Difficult data analysis & interpretation*
- *The challenge was to find an accelerated stress test method that solved the above concerns.*

ALTERNATIVE TEST METHODS COMPETITIVE ANALYSIS

Element	Thermal Cycling	Liq/Liq	Fluid Sand	Solder Float
Test Type/Temp	Stress (-65/+125C)	Shock (-35/+125C)	Shock (25-260C)	Shock (25-260C)
Characterization	Difficult	Fair	Fair	Difficult
Time to Results	288	120	2	.5
Cost of Test (/100 cyc.)	$275.00	$160.00	N/A	N/A
Cost of Ownership (5 yrs)	$175K	$110K	$45K	$10K
Data Collection	additional @$10K	additional @$10K	additional @$10K	N/A
Installation	Hard wired Drainage, Compressed Air	Hard wired Drainage, Compressed Air	Hard wired Drainage, Compressed Air	Requires Exhaust
Environmental	Nitrogen/CFC's	CFC's	Emits Lead	Emits Lead

COMPETITIVE ANALYSIS

ELEMENT	IST	Thermal Cycling	LIQ/LIQ
Test Type/Temp	Stress (25-150C)	Stress (-65/+125C)	Shock (-35/+125C)
Characterization	Easiest	Difficult	Easier
Failure Detection Cost of Ownership	Early detection $98K	Not applicable $175K	Not applicable $110K
Cost of Test (/500cyc)	$65.00	$375.00	$320.00
Data Collection Capabilities	Integrated PTH + Post	Additional @10K PTH	Additional @10K PTH
Time to Results (hrs)	24	288+	120
Installation Mass-Microsectioning Environmental	Portable AC Outlet No Friendly	Hard wired Drainage, Compressed Air Yes Nitrogen/CFC's	Hard wired Drainage, Compressed Air Yes CFC's

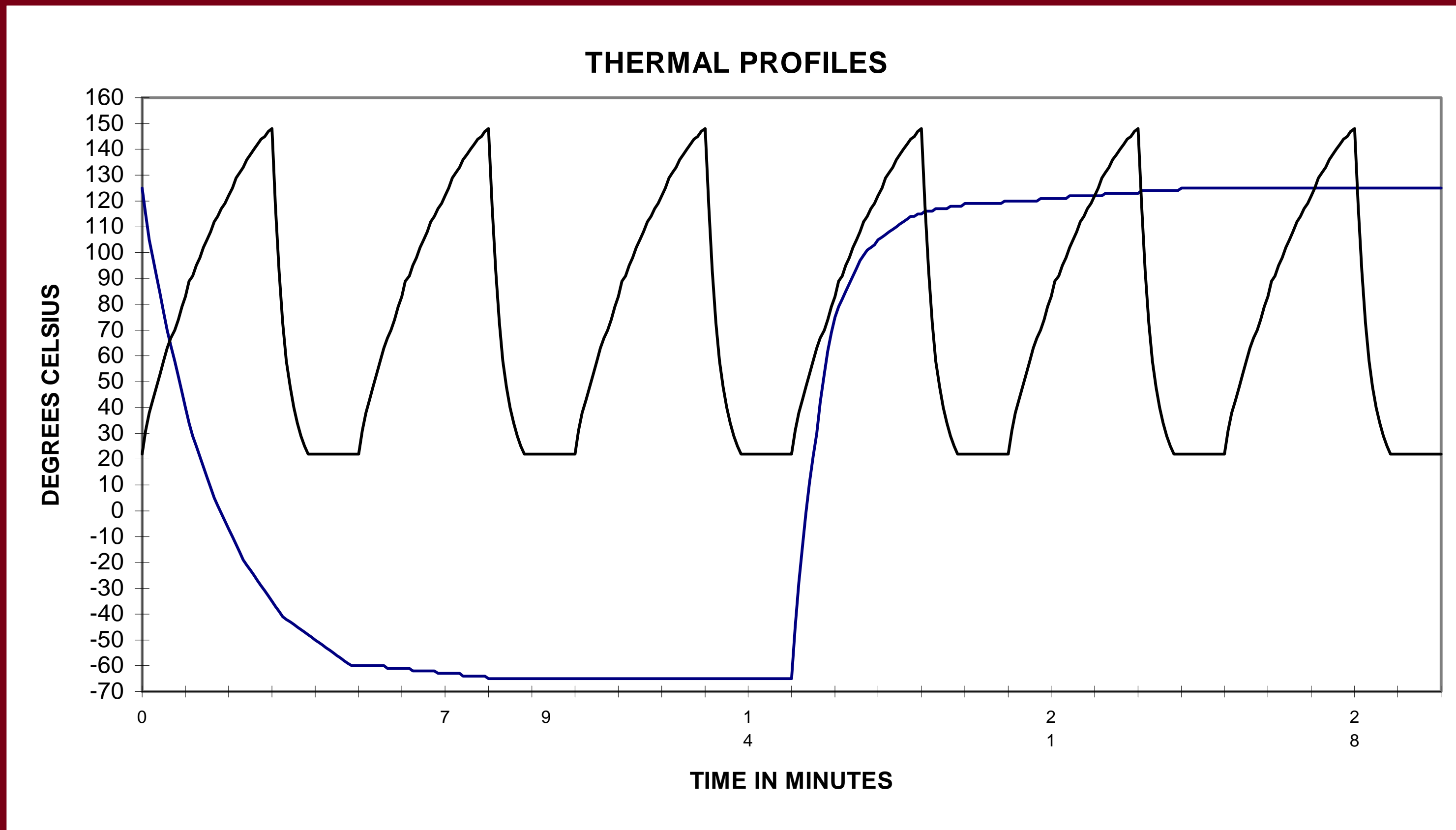
DISTINGUISHING ATTRIBUTES OF I.S.T. Compared to Traditional Methods

- *Test 2 separate areas of same interconnects*
- *Identifies failure hierarchy/interactions*
- *Quantifies severity of process defects*
- *Speed - 6X faster (minimum) than T.C.*
- *User friendly - Automated process*
- *Low operating/maintenance cost*
- *No stressing beyond failure criteria*
- *No consumables (Nitrogen/Chemicals)*
- *Reduces extensive micro-sectioning*
- *Excellent repeatability/reproducibility*

DISTINGUISHING ATTRIBUTES Compared to Traditional Methods

- *Operator independent*
- *Flexible test parameters*
- *Capable of creating isolated thermal zones (related to coupon circuit design)*
- *Data collection and analysis integrated*
- *Immediate use ("Plug and Play")*
- *Weakest link in the chain identified*
- *Floor space optimized / Portability*
- *Highly reliable*

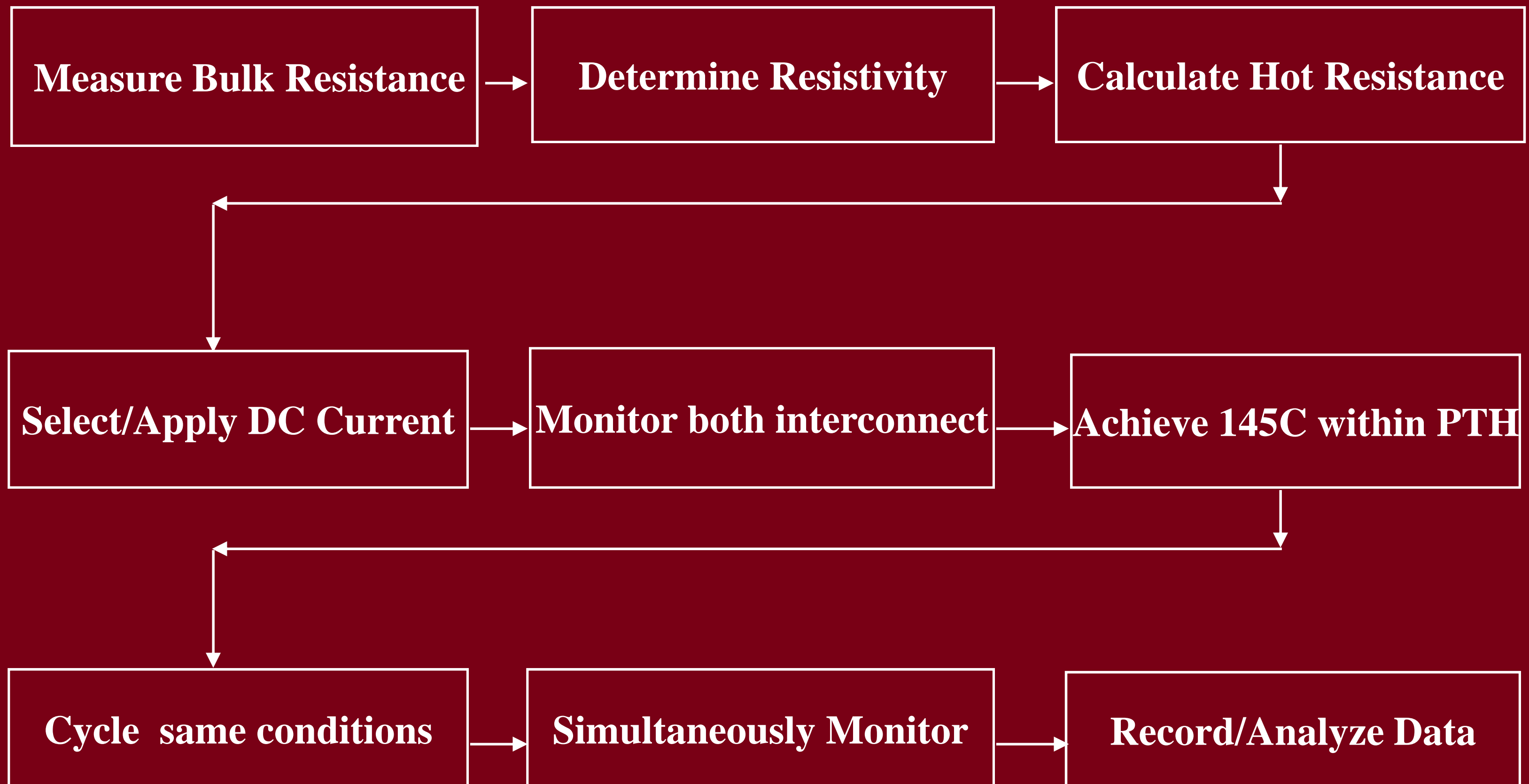
Profiles of I.S.T. and Air to Air Thermal Cycles



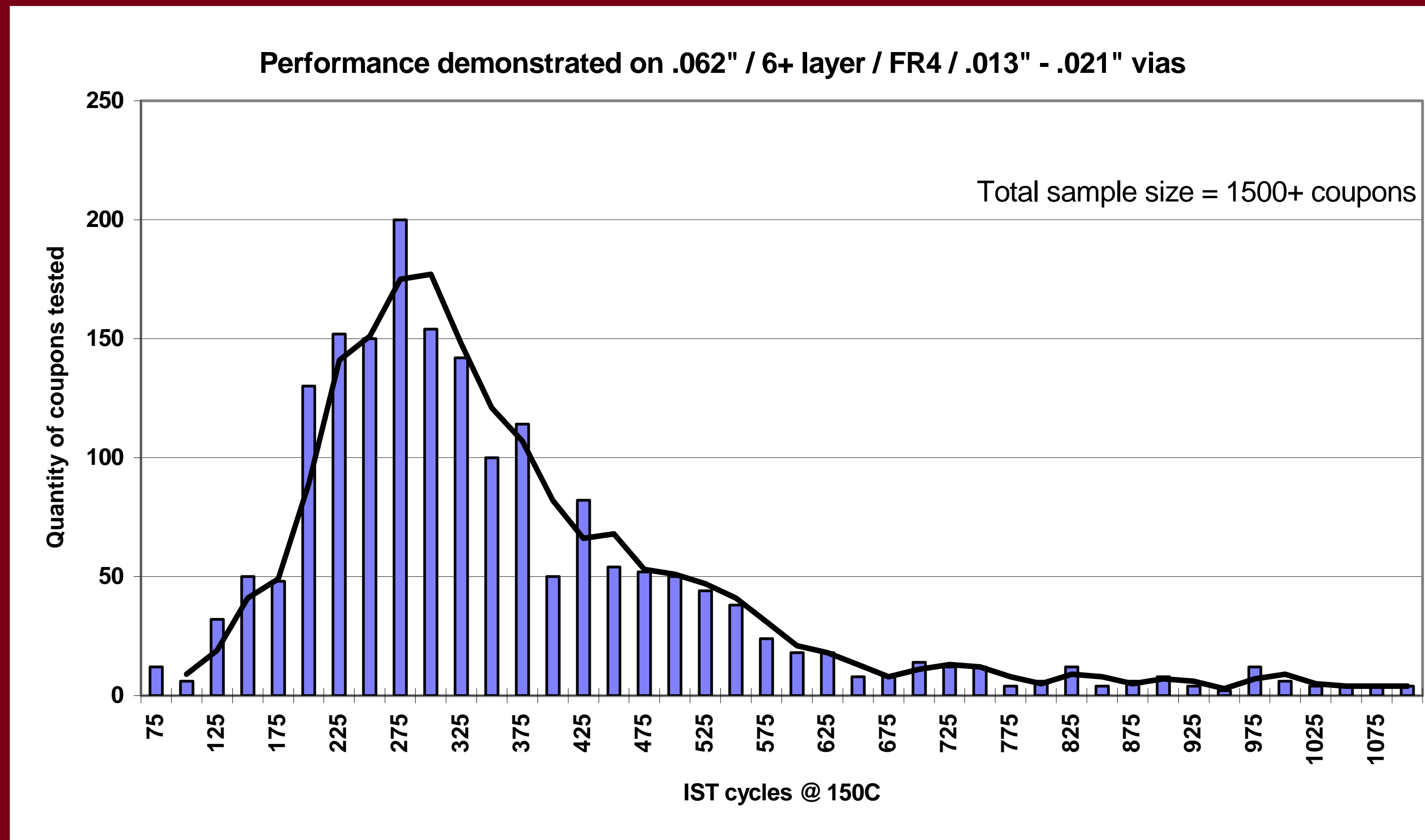
I.S.T. PRINCIPLES FOR PTH and POST INTERCONNECT TESTING

- *Apply DC current to internal interconnect, monitors & controls resistance/temperature through PTH interconnect. (eg. 145C +/- 2C in 3 minutes).*
- *Differential thermal expansion continues until failure inception initiates as micro-structure cracking, located in specific regions within one or multiple areas of the interconnect.*
- *Cycling continues until the specified rejection criteria is achieved.*
  - *10% increase in PTH/Post interconnect*

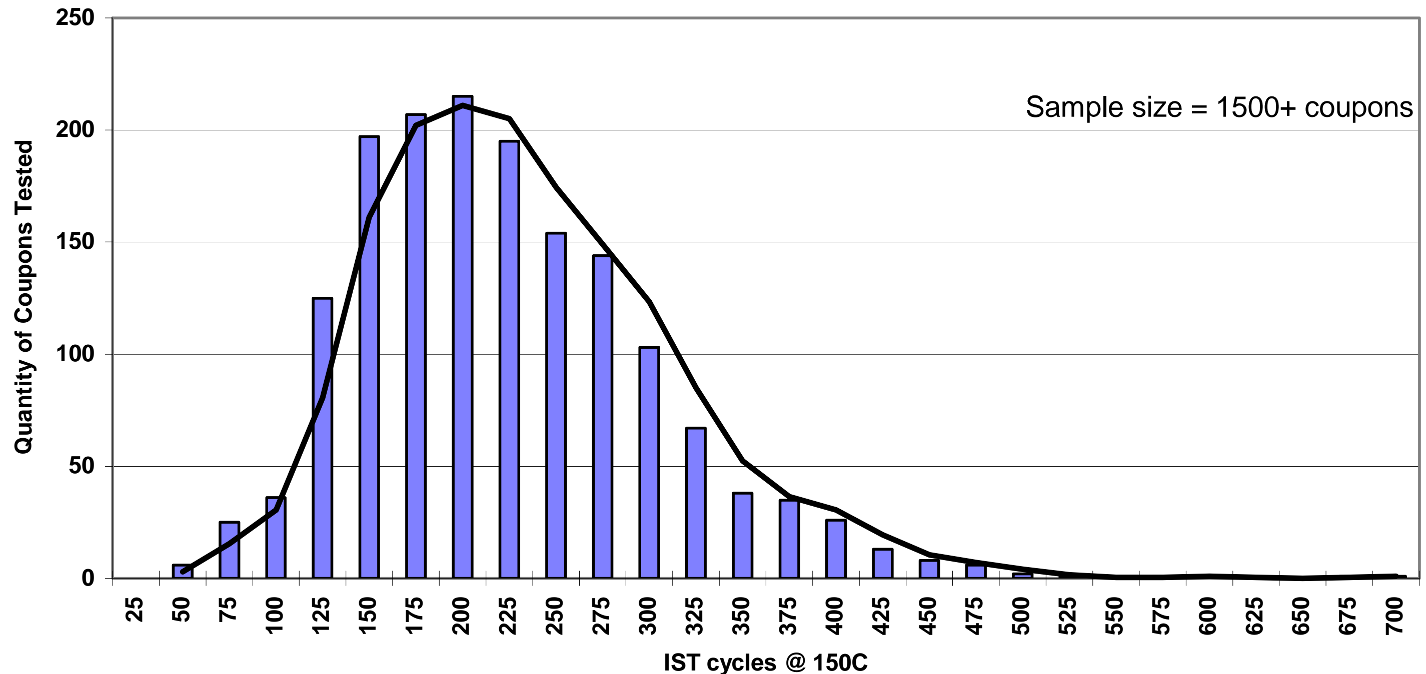
Test Methodology
I.S.T. Automated System Sequence



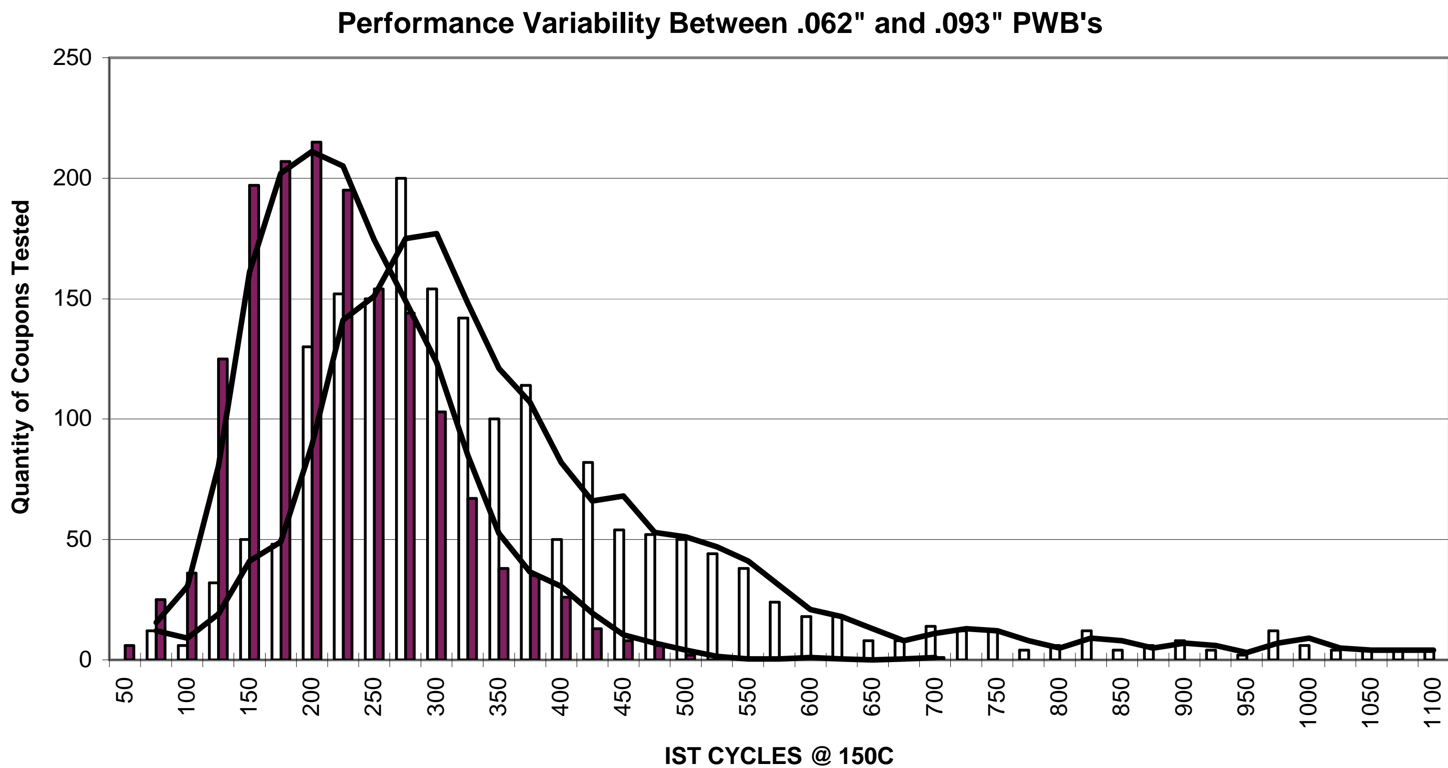
Performance Variability of Similar .062” Technologies



Performance variability of Similar .093" Technologies



Performance Variability of Different Thickness PWB's



Resistance Degradation for Traditional Technologies

INTERCONNECT PERFORMANCE ON I.S.T.

.062" / 6 TO 10 LAYERS / .013" TO .021" VIAS / .0012" COPPER / FR4 MATERIAL

RESISTANCE CHANGE IN MILLIOHMS
50
45
40
35
30
25
20
15
10
5
0

HIGH QUALITY INTERCONNECT

INCREASED RELIABILITY

1 22 43 64 85 106 127 148 169 190 211 232 253 274 295 316 337 358 379 400 421 442 463 484 505 526 547 568 589

IST CYCLES @ 150C

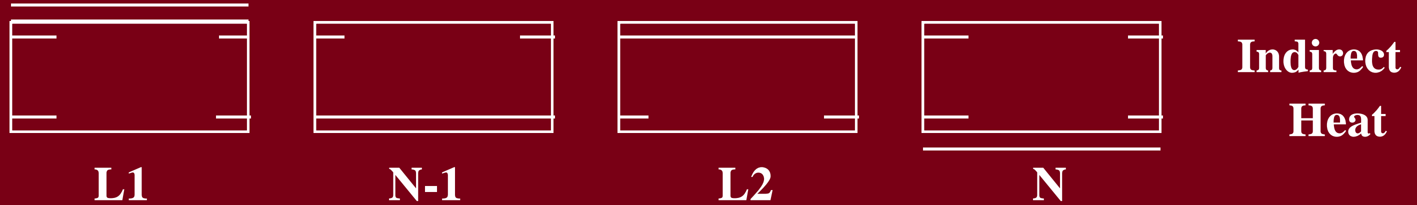
PTH Vs Post Interconnect Baseline Test Coupon Design

- *Post Interconnect :- 200 Daisy chain vias, interconnecting through 2 adjacent layers (Lyrs 2&3 / N-1&N-2)*
- *Minimize dielectric spacing to reduce interference from PTH barrel failure zones (.006" - .008" optimum)*

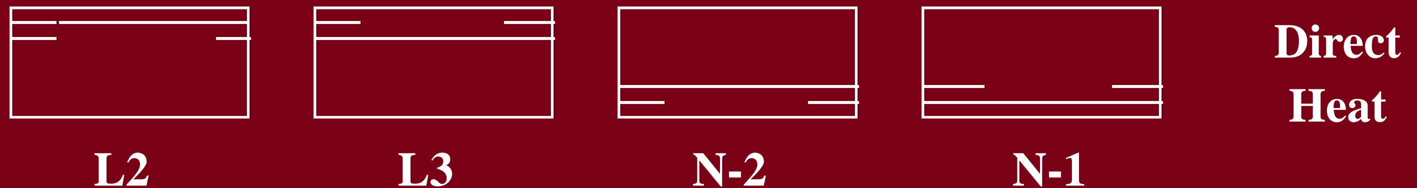
- *PTH Interconnect :- 2 (parallel resistor) independent daisy chains, interconnecting 500 vias through any 2 inner layers at various levels within the PWB (Lyrs 1&7 2&6 / 3&5 Etc)*
- *PTH Interconnect runs parallel to Post interconnect*

INTERCONNECT DESIGN
PTH/Post Test Coupon

PLATED THROUGH HOLE INTERCONNECT (Small via)

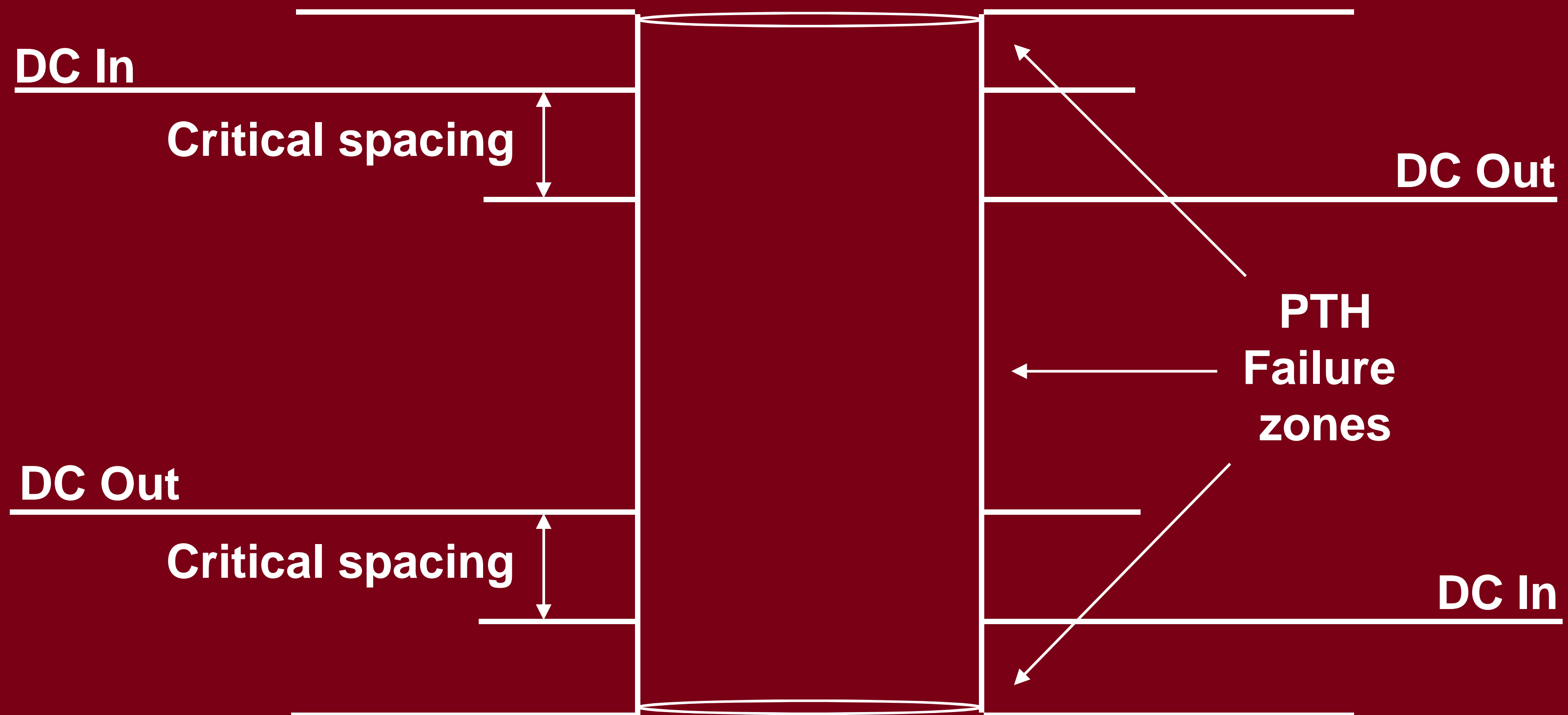


POST INTERCONNECT (Large via)



I.S.T. coupon construction for post interconnect testing

Dielectric spacing between layers 2/3 and N-1/N-2 should not exceed .010”



Correlation studies

DEC	Thermal Ovens - Mil Std 55110D - Microsection/SEM
Circo Craft	Thermal ovens (Delco1000HR) - Liquid to Liquid Sand bath - Solder float - Microsection - SEM
IPC/PTV	Thermal Ovens - Liquid to Liquid - Sand Bath CITC -MicroSection
IPC/EPA	Microsection - SEM
Nelco Tech	Thermal Ovens (Delco 1000HR) - Microsection
Delco	Thermal Ovens (Delco 1000HR) - Different Oven temperatures - Microsection
NASA	Microsection
Merix Corp.	Microsection - SEM
Electrochem	Liquid to Liquid - Microsection
Motorola	Liquid to Liquid - Microsection
Shipley	Thermal Ovens - Mil Std 55110D - Microsection
Honeywell	Thermal Ovens - (1000HR) - Microsection
Compaq Computers	Liquid to Liquid - Microsection

Repeatability and Reproducibility of I.S.T. Testing

- *System Specification/Conditions*

Resistance measurement accuracy = +/- 2.5 milliohms

Temperature accuracy = +/- 5 % (+/- 3 degrees C)

Cycle time accuracy = + 3 seconds / - 0

Calibrator (precision resistors) = +/- .5 %

Monitoring - Continuous and simultaneous on both interconnects

Repeat testing - Test conditions saved in system memory

Quantity - 6 coupons customized to same thermal profile

Functions - Automatic

Failure Detection using Old and New Test Methods

- **Microsectioning:**
  - Low number of holes tested
  - Evaluates 1 degree of holes circumference
  - Go / No Go test
  - Poor repeatability
  - Operator dependent
  - Visual criteria

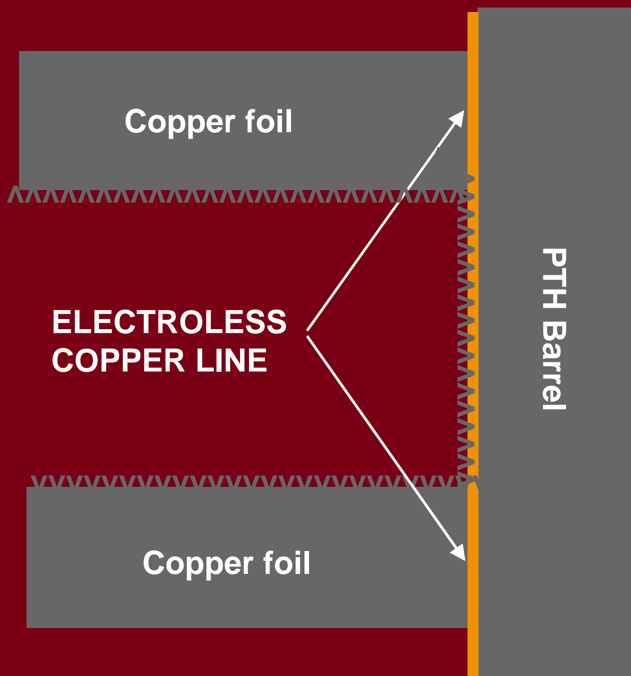
- **IST Testing:**
  - High number of holes tested
  - Evaluates 360 degrees of all connections
  - Quantifies severity
  - Excellent repeatability
  - Operator independent
  - Electrical criteria

Critical Factors Influencing the Detection of Post Separation

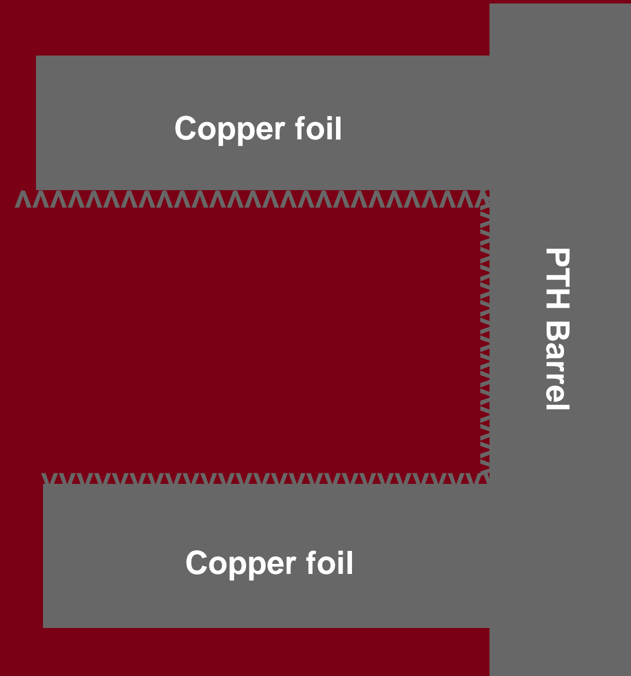
- **Microsectioning:**
  - Sample conditioning
  - Potting Compound **
  - Grinding ***
  - Polishing ****
  - Etching
  - Interpretation

- **IST Testing:**
  - Coupon Design
  - Interpretation

Comparing Connections to the Innerlayers

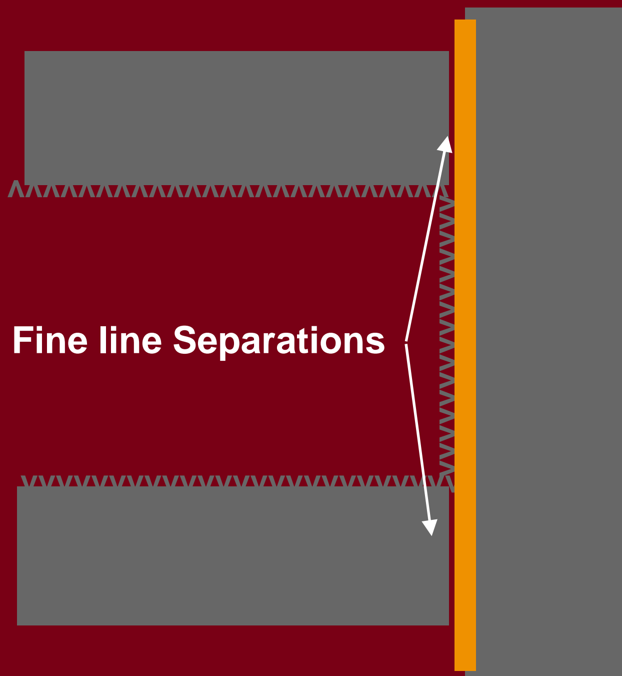


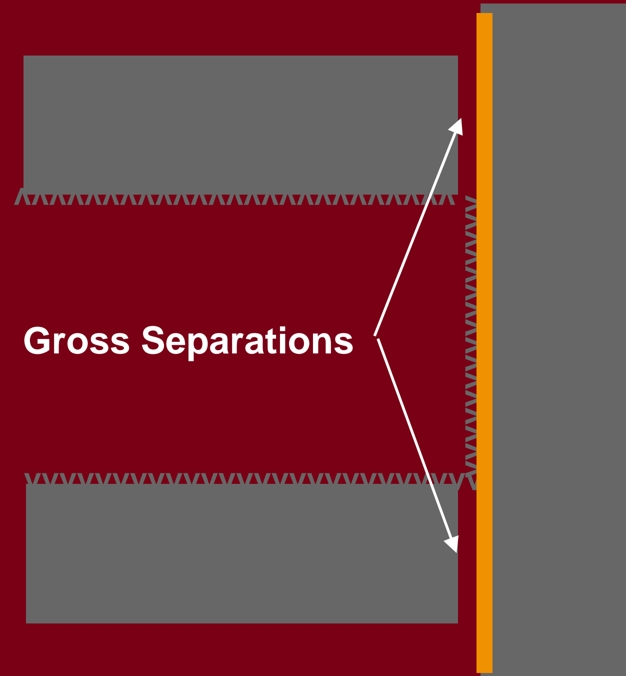
Traditional Electroless Copper



Direct Metallization

Defects Found with Connections to Innerlayer

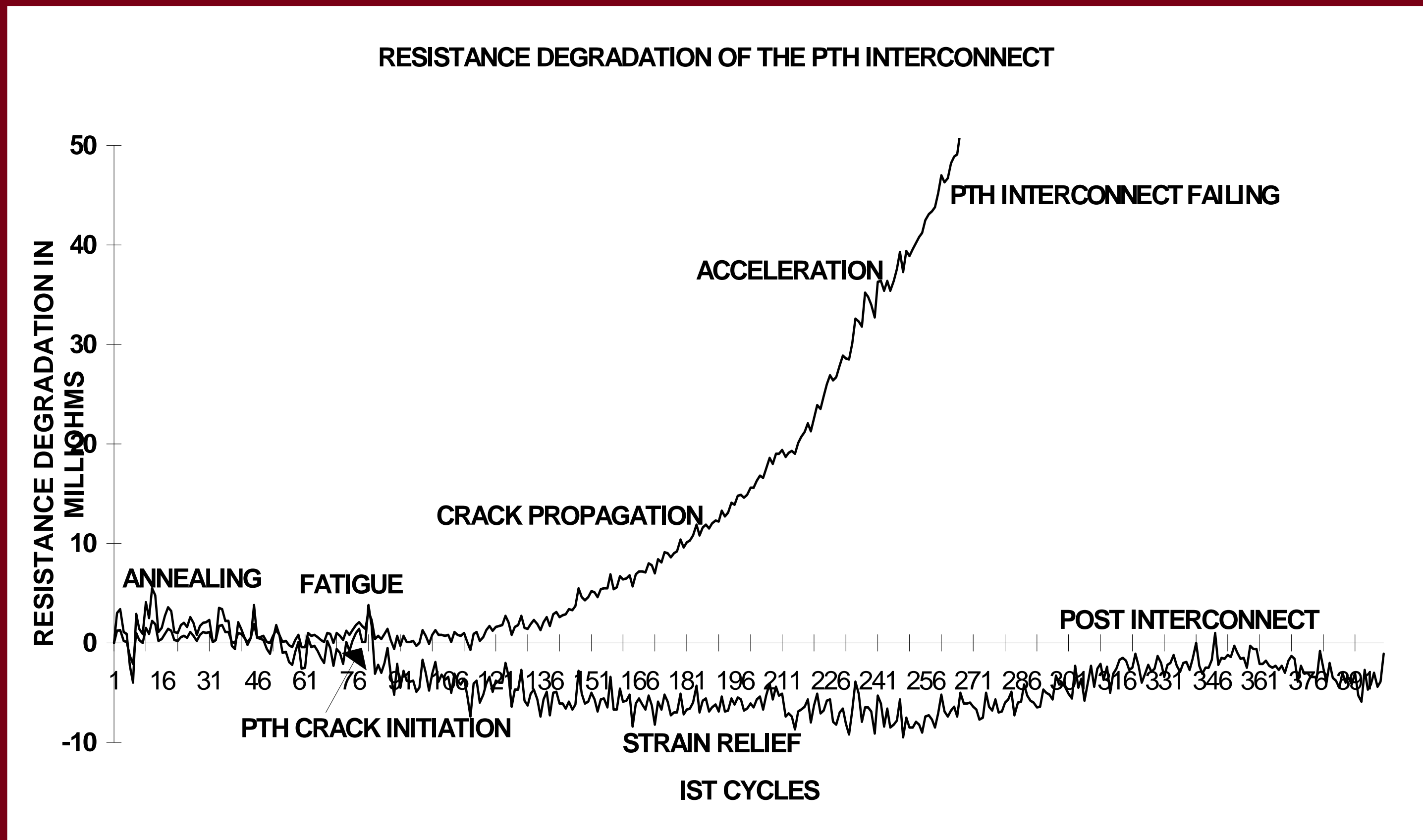




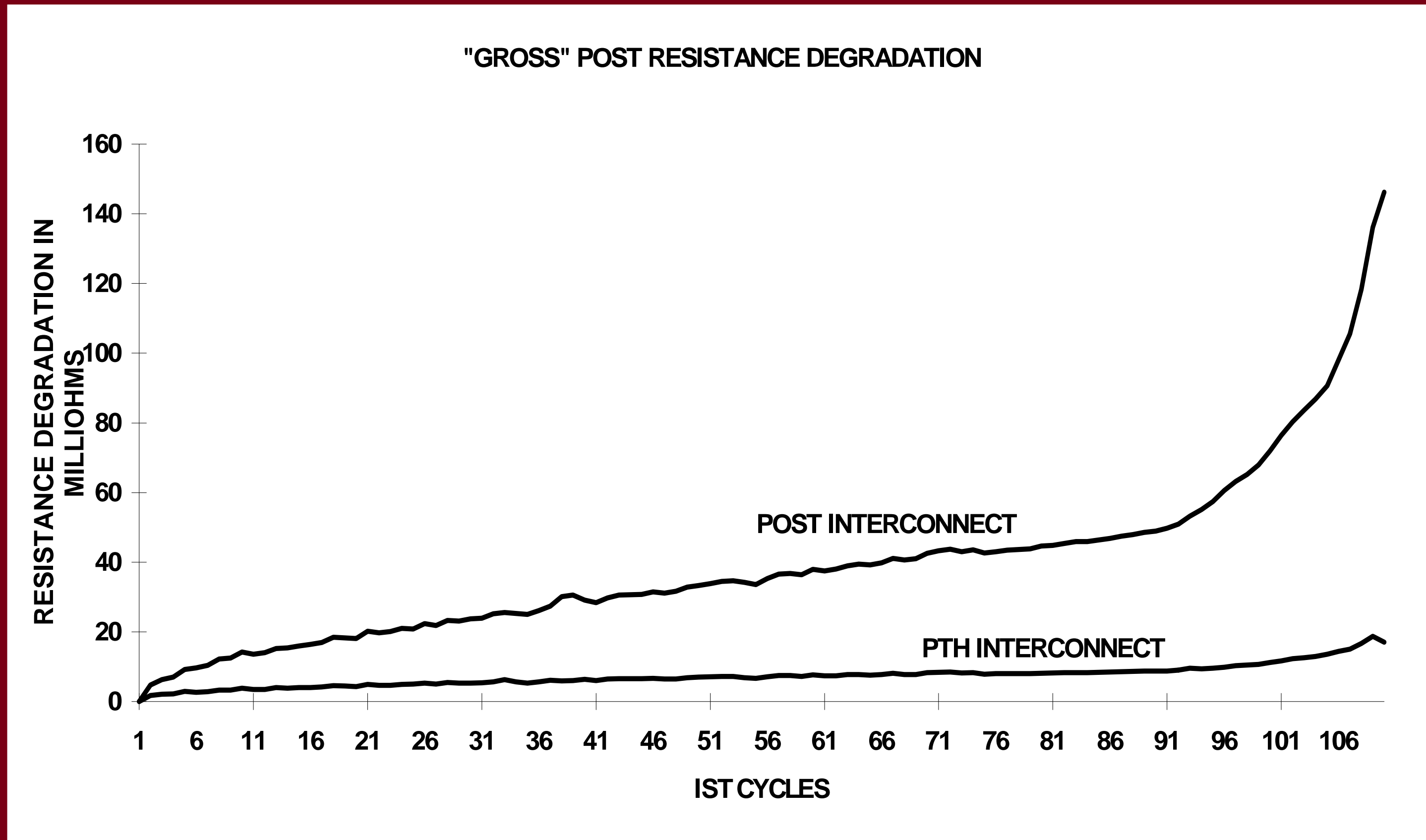
“Phase’s of Damage Accumulation”

- *Annealing :- Initial strain relief due to mechanical stressing of the interconnect*
- *Fatigue :- Influence of mechanical strain*
- *Crack initiation :- Micro-structure cracking within the interconnect (specifically the PTH or inner layer interface)*
- *Crack Propagation :- Micro-cracks combining to develop semi-cylindrical cracks*
- *Acceleration :- The coalescing of micro-cracks to form fully cylindrical cracks*
- *Strain Relief: The adaptivity of the PWB to redistribute the strain*

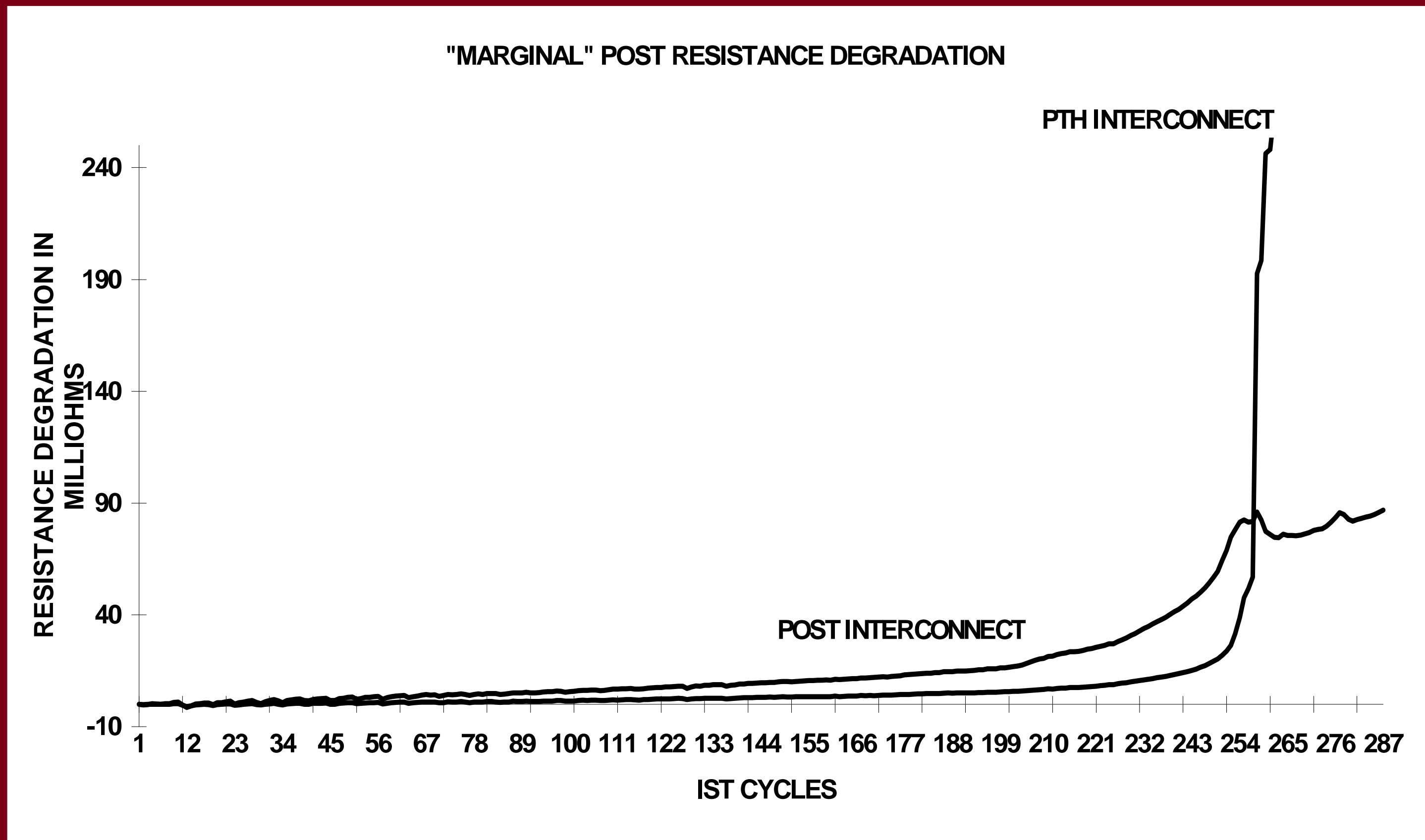
Resistance Degradation of the Interconnect



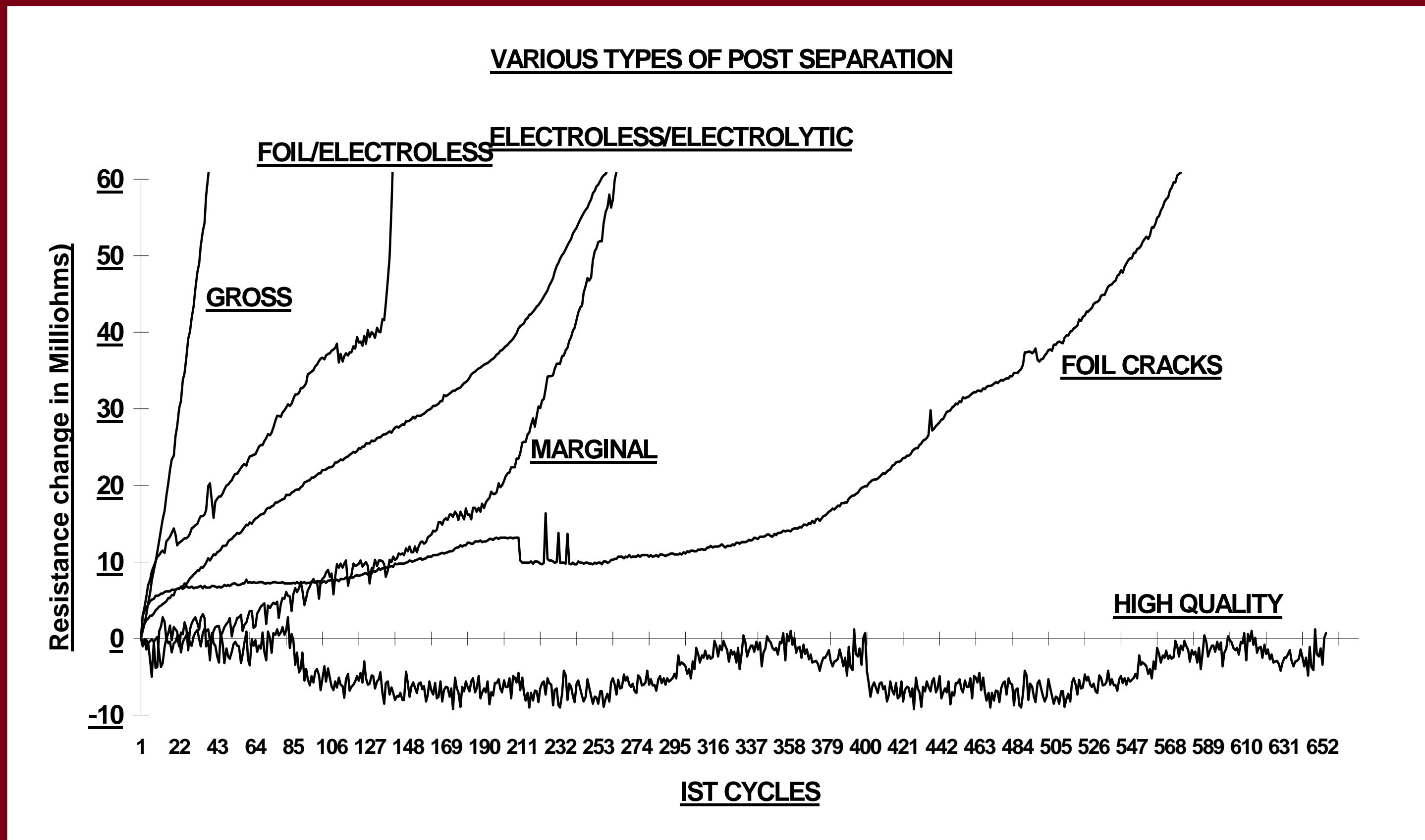
Post Separation Creates Independent Interconnect Failures



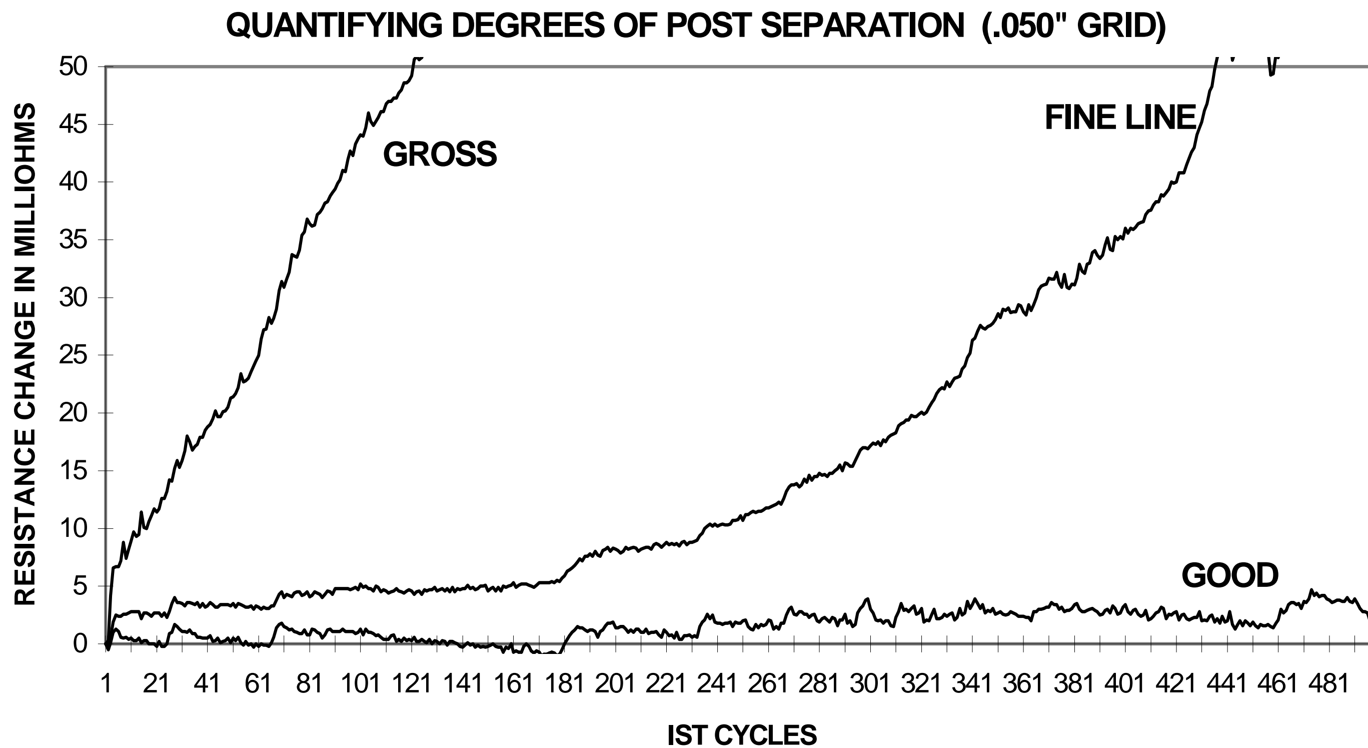
Dominant Vs Latent Failure Hierarchy



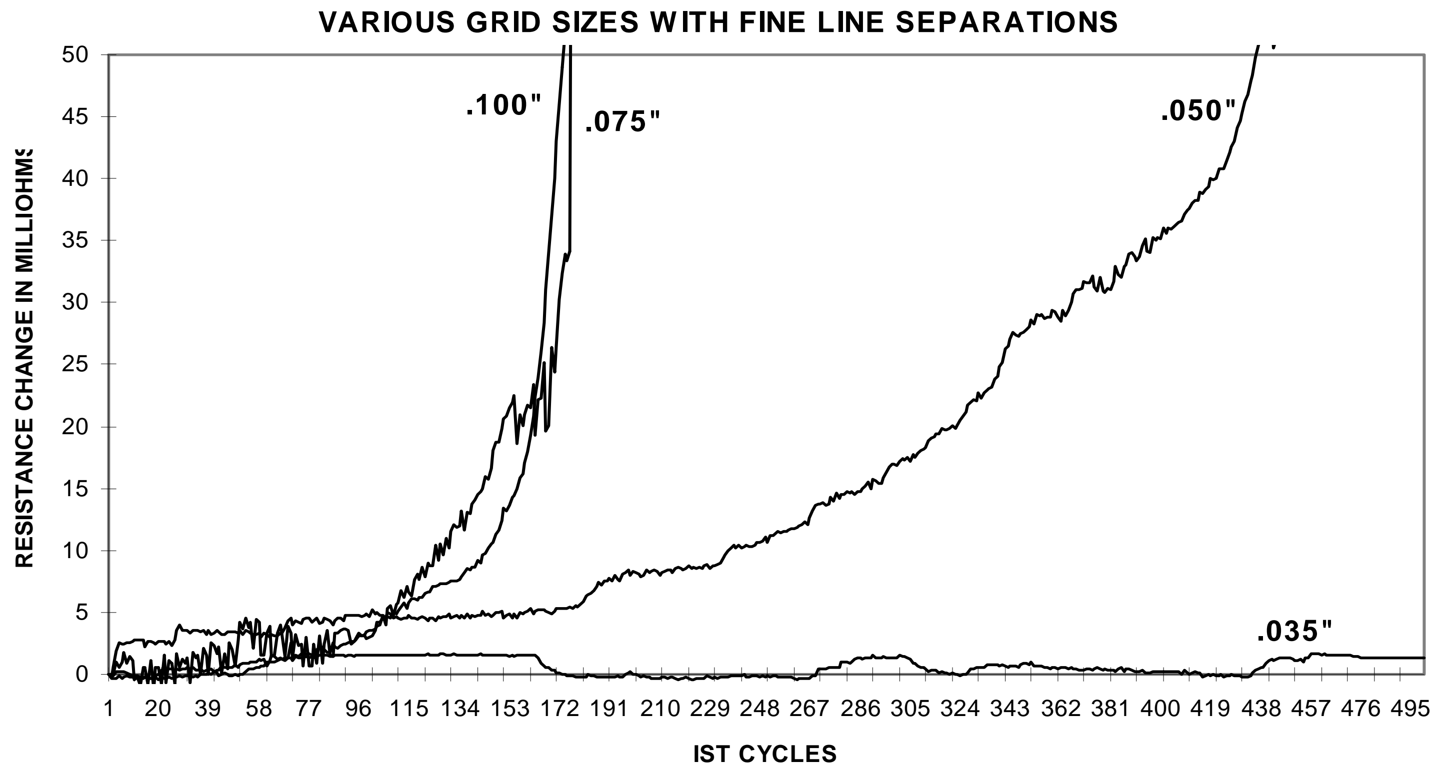
Levels of Interconnect Failure



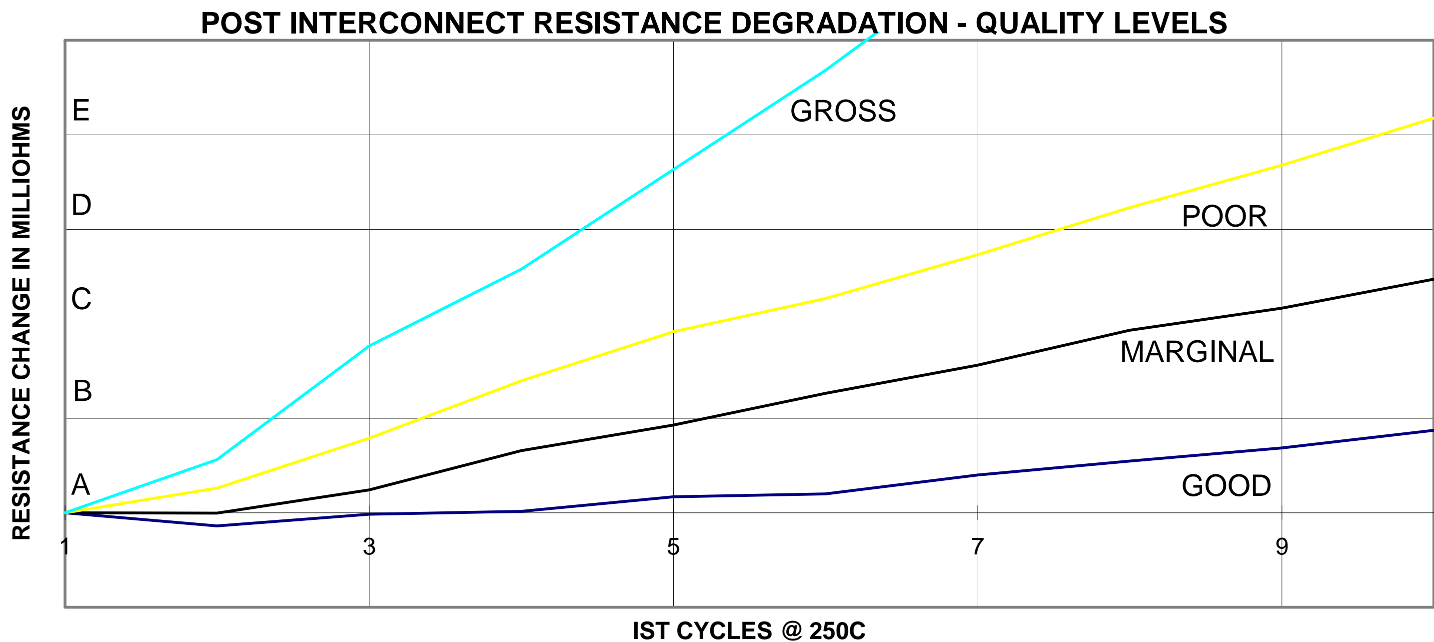
Electrically Testing for Post Separation



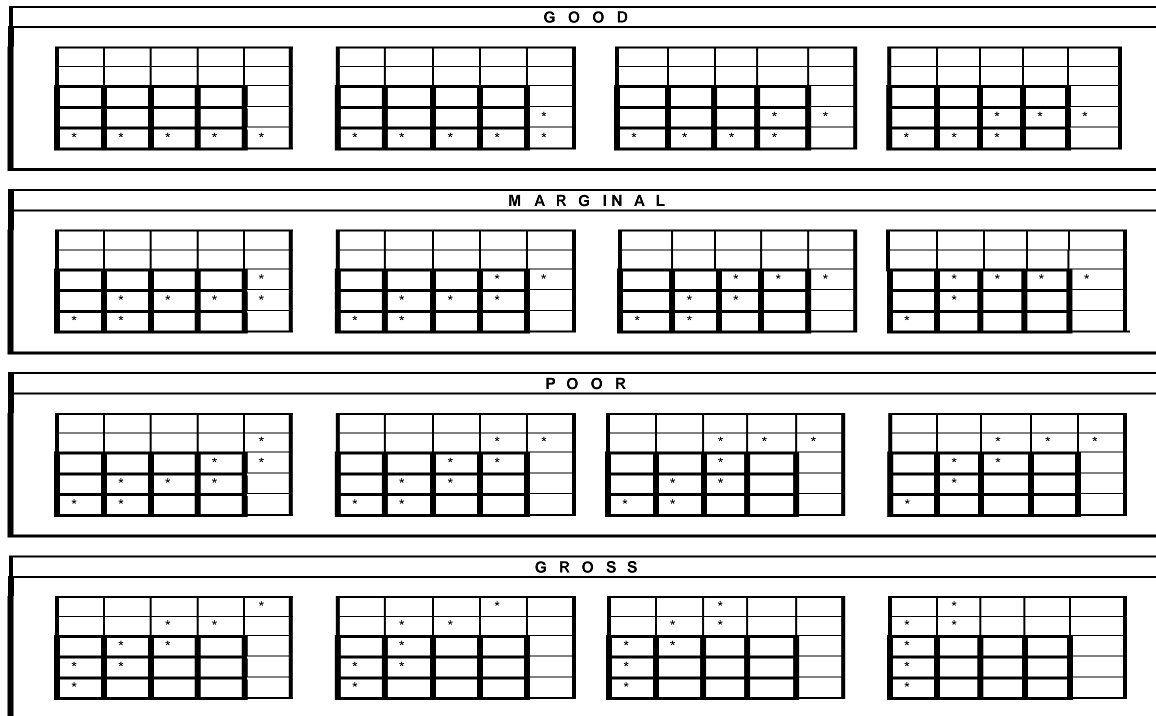
Influence of Grid/Hole Size to Precipitate Post Separation



“Levels” of Post Separation



Associated Vectors



Activities with the I.P.C. and I.S.T. Partners

- *Completed repeatability and reproducibility studies with multiple IST users and traditional test labs*
- *Determine the applicability of the I.S.T. approach to effectively quantify the presence and influence of post separation on PTH interconnect reliability*
- *Establish impact of various assembly conditions on long term reliability of total interconnect*
- *Review ongoing performance/development efforts at IPC committee meetings*
- *IST technology selected as test method to quantify via registration & reliability of Micro-via technologies (ITRI)*