C99-51

Evaluation of IST

D.B. Barker and M.D. Blattau,

Kevin Cluff (Honeywell)

Objective: *To develop a finite element model to understand interconnect stress testing results and to relate them to oven chamber testing and field usage.*

What is IST?

- IST is an acronym for the Interconnect Stress Testing procedure.
- Uses current flow to thermally stress the PTH's within a printed wiring board assembly.
  - PTH's (printed through holes) electrically connect one layer to another.
  - IST tests the integrity of these interconnects.
- Helps determine whether the printed wiring board assembly can withstand the rigors of the manufacturing process and end use environment.
- Rapid assessment or comparison between various board manufacturers and/or plating.

Terminology Trends

re: IPC Technet Discussions

PTH (Plated Through Hole)	→	PTV or PTH/PTV (Plated Through Via)
Post Separation	→	IL Separation (innerlayer separation)

IST - History/Background

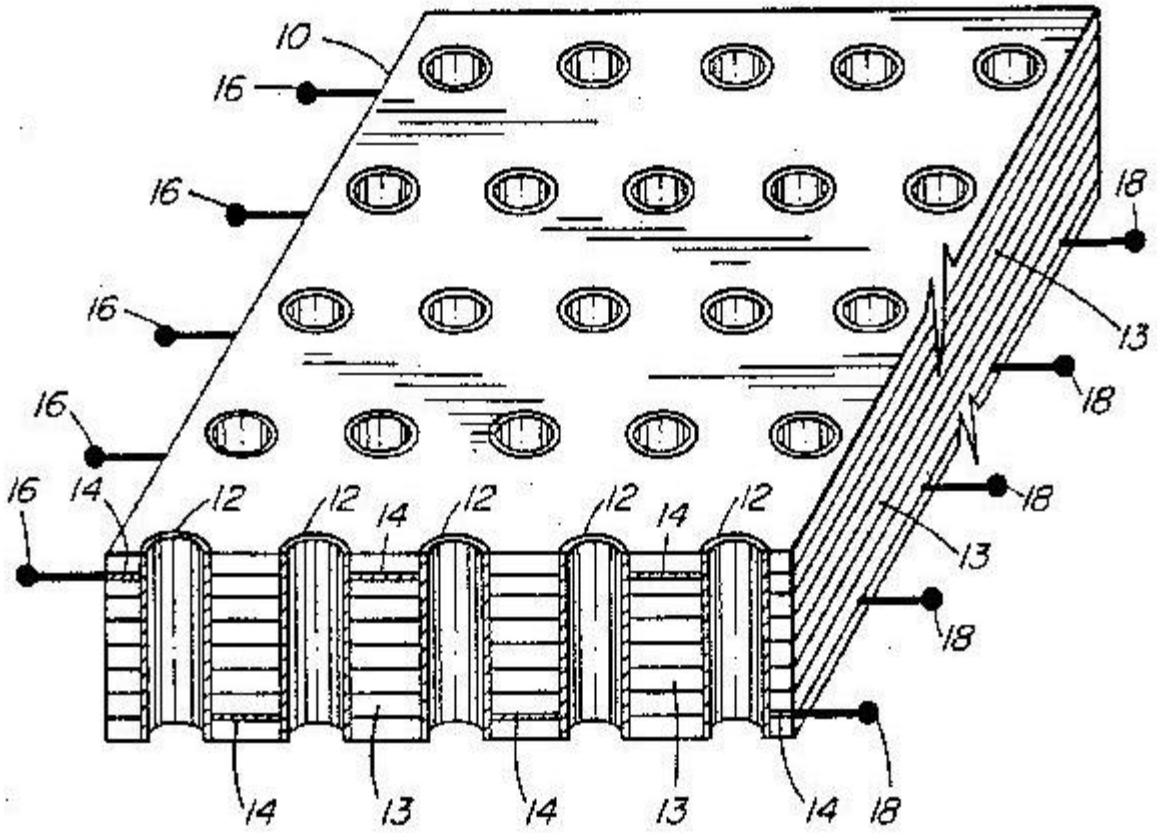
- PCT (Power Cycling Technique) developed by Northern Telecom in 1987
- Research into the repeatability and reproducibility of PCT continued in a 1989 joint venture between Northern Telecom and Digital Equipment Corporation.
- After poor results/correlations the project is dropped by Northern Telecom and continued solely by Digital.
- New principles are developed at DEC as well as new coupon designs and the name changed to IST.
- In September 1995 a patent is submitted for IST.
  - Inventors: Stephen M. Birch, Gerald M. Gavrel, and Zaffer I. Memom
  - Assignee: Digital Equipment Corporation
- Licensed to PWB Interconnect Solutions, Inc.
  - Provides complete IST systems
  - Continues researching various coupon designs
  - web page: www.pwbcorp.com
- IBM still working on CITC (Current Induced Thermal Cycling), which is similar to the PCT concept.

IST vs. PCT

- PCT (Power Cycling Technique)
  - Uses ohmic heating to heat the holes, interconnects, and surrounding substrate to a temperature above the boards glass transition temperature.
  - Cannot distinguish between post separation failures and barrel cracking.
  - Non-uniform board heating (hot spots).
- IST (Interconnect Stress Testing)
  - Includes separate post-interconnects and barrel circuit
  - Uses ohmic heating through the post-interconnects only, to heat the substrate uniformly.
  - Continuously monitors resistance changes in both the post-interconnect circuit and in the barrel test circuit.

PCT Coupon Design

Heating Current is Passed Through Every PTH

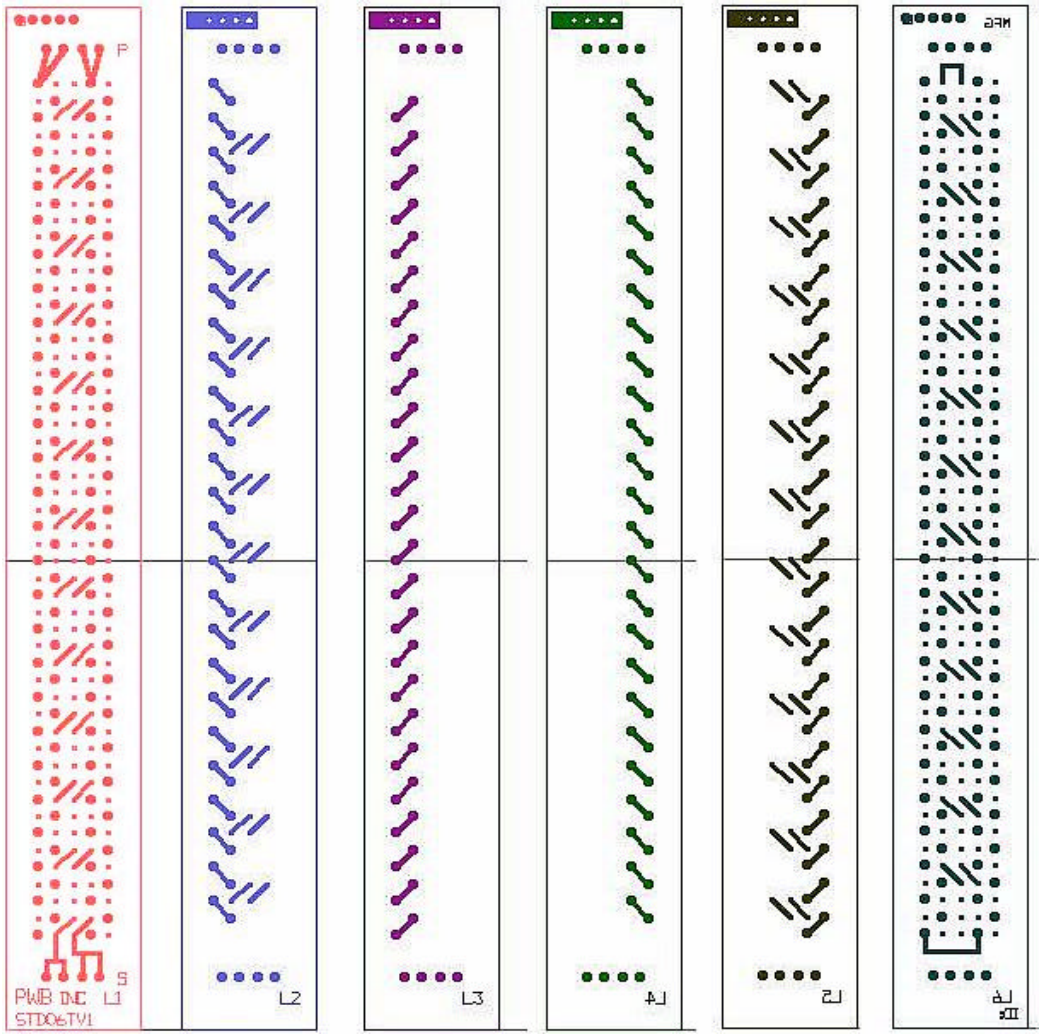


Plated Areas of a 6 Layer IST Test Coupon

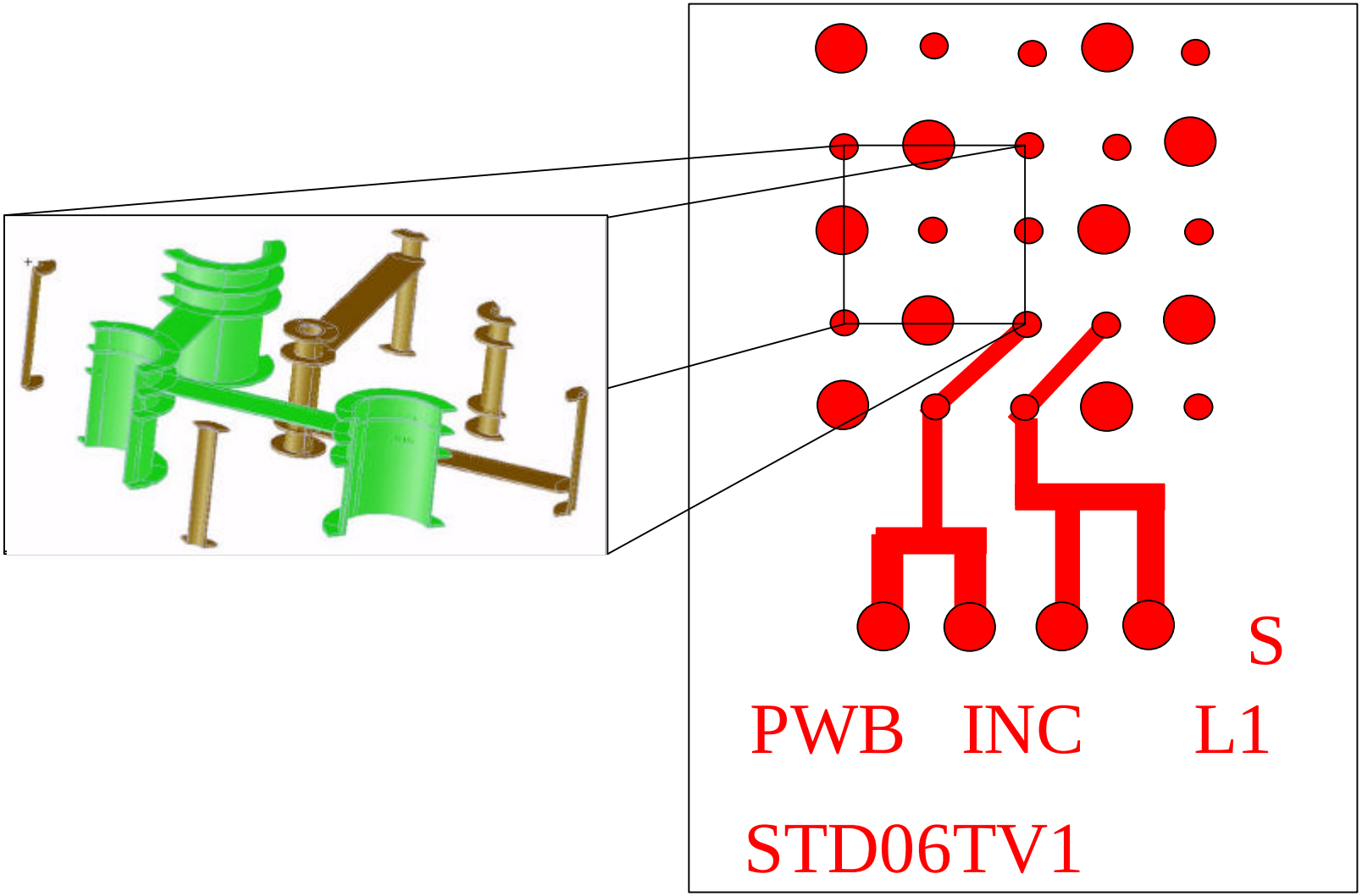
(Recent Coupon Design from PWB Interconnect Solutions, Inc.)

IST Coupon Design

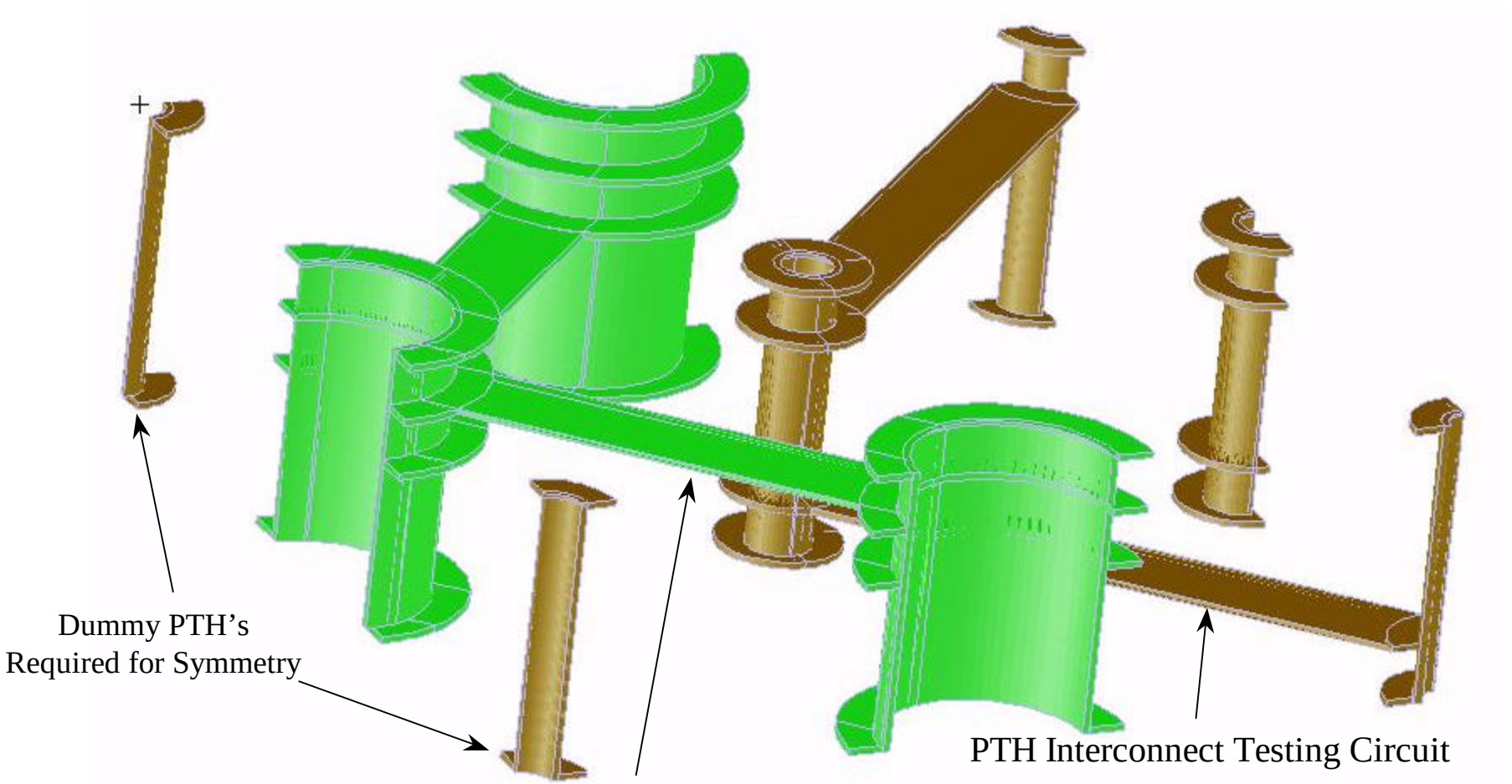
- Distance between holes 0.1”
- PWB thickness 60 mils - 93 mils
- 6-16 layer PWBs
- Plating thickness 0.5 mils - 2 mils
- Electroless/Direct metalization or other
- Designer: PWB Interconnect Solutions, Inc.



Sample Detail of Vias and Traces



Example of 6 Layer Layout



Interconnect Stress Testing Cooling Chamber Design and Coupon Layout

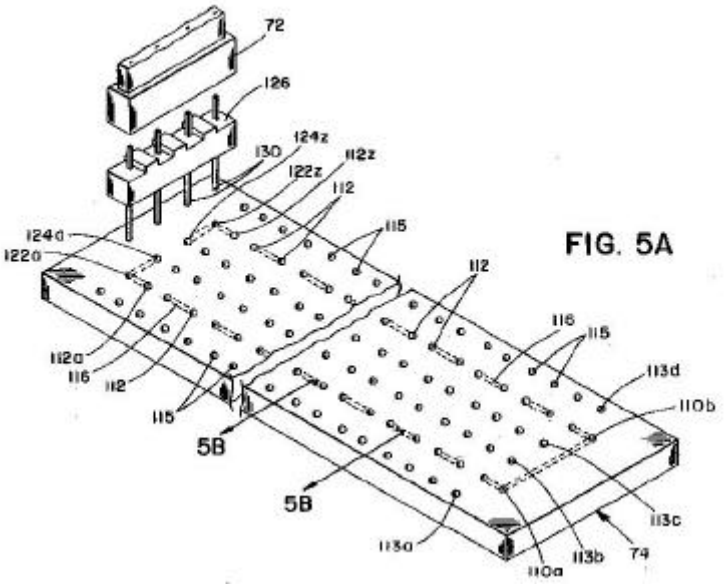


FIG. 5A

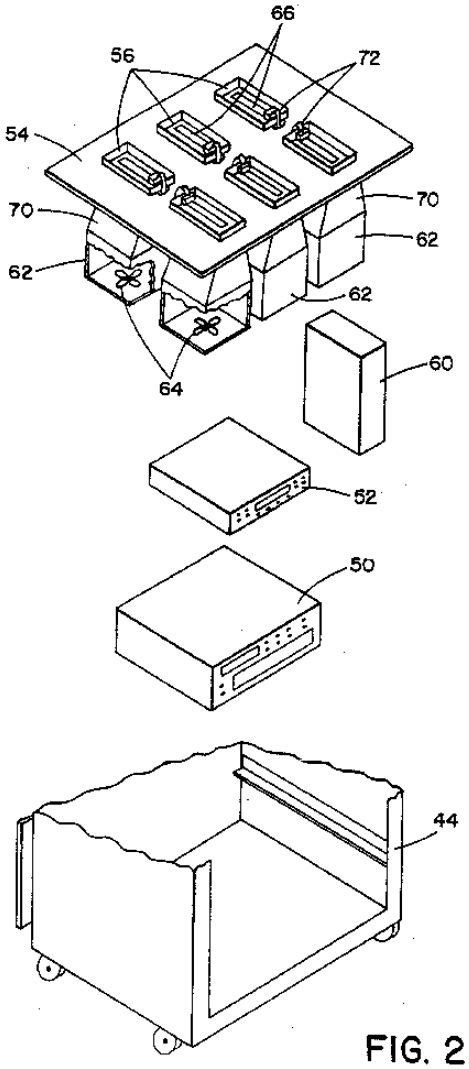
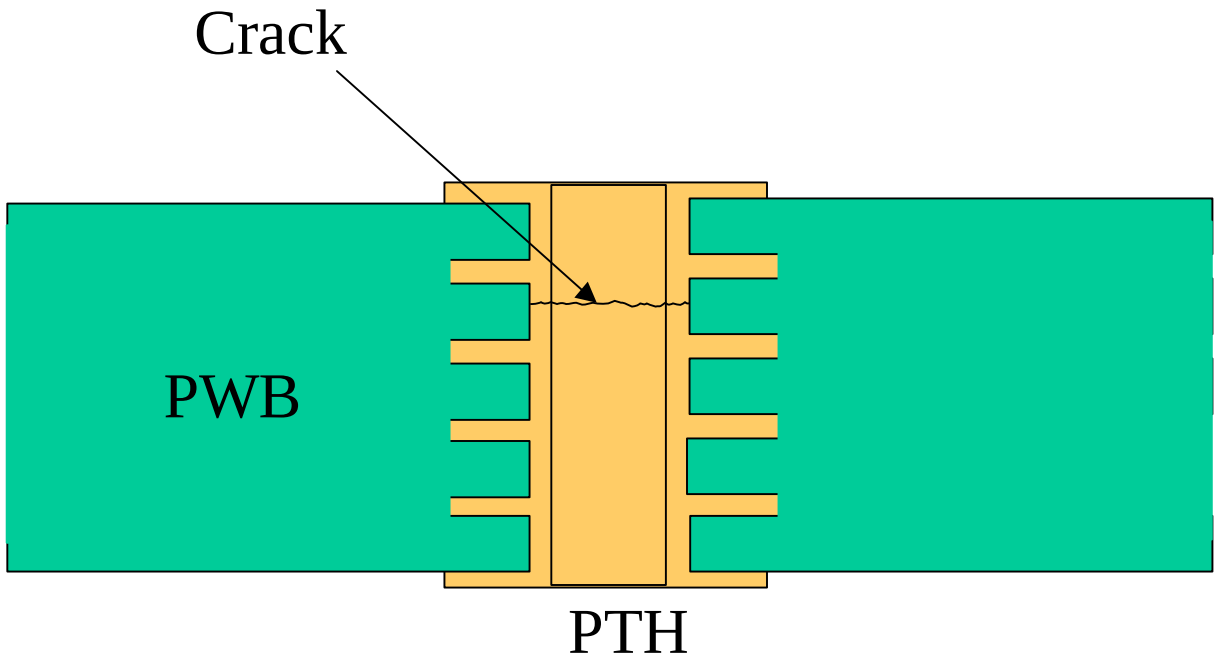


FIG. 2

Barrel Failure

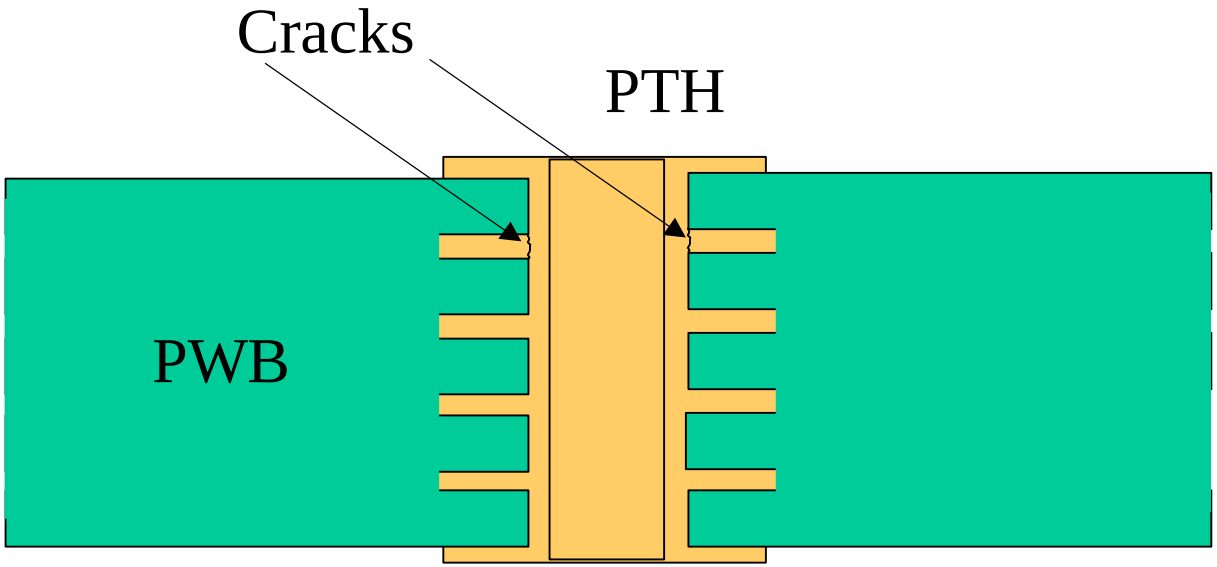
circumference cracking of barrel



- More common in high aspect ratio holes
- Dependent on plating quality

Post Cracking

foil pad-barrel interface cracking (IL - inner layer separation)



- Separation of barrel from surrounding inner-layer
- Corner cracks
- Usually found in low aspect ratio holes
- Highly dependent on plating quality

IST Pre Cycling Test Sequence

From IPC-TM-650

"DC Current Induced Thermal Cycling Test"

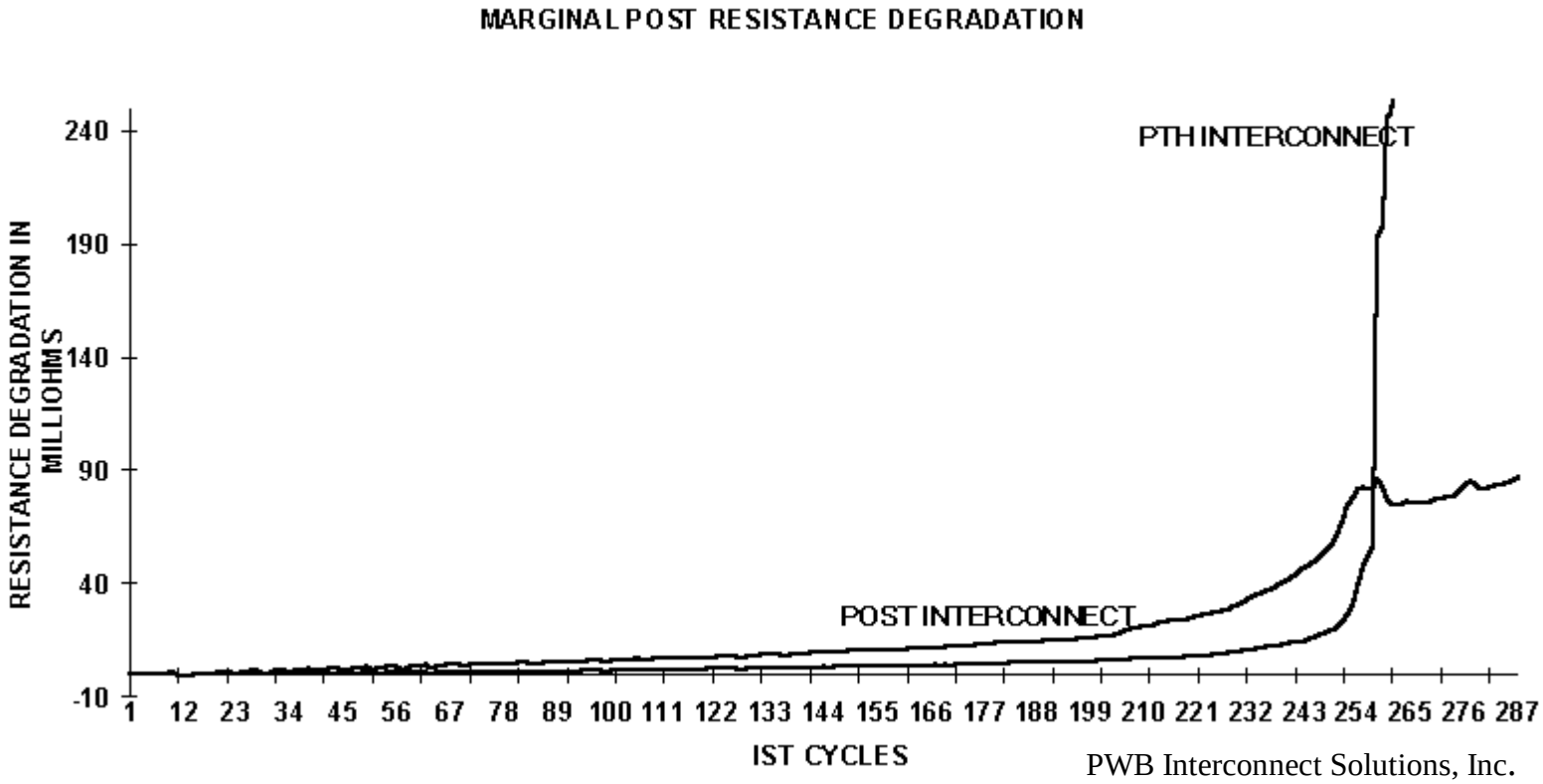
- Ambient Resistance: Auto ranging multi-meter measures the ambient resistance of the coupon's heating circuit.
- Target Temperature Resistance: The system software calculates and displays the required "target" resistance (temperature).
- Rejection Resistance: The rejection resistance is calculated and displayed. This is added to the target resistance to establish the rejection criteria.
- Current: The system selects an initial current based on the ambient resistance of the coupon. During pre-cycling the initial current is adjusted so that the target resistance (temperature) is achieved in 3 minutes.
- Pre-cycling initiated by application of initial current. The system then checks the resistance after 3 minutes to see if the target resistance is achieved. If not the system adjusts the current and pre-cycles the coupon again.

IST Stress Cycle Test Sequence

From IPC-TM-650
"DC Current Induced Thermal Cycling Test"

- Initiation of stress test by applying current determined by pre-cycling for three minutes. After three minutes the coupon is cooled for 2-3 minutes depending on the thickness.
- Coupons are repeatedly cycled until one of the rejection criteria are achieved or the maximum number of cycles is completed.
- The coupon's resistance increases as failure inception occurs. The rate of change in the resistance is analogous to the degree of mechanical failure.
- When the coupon's resistance exceeds the rejection resistance the IST stress testing is stopped. This rejection criteria prevents thermal runaway.
- The IST systems continuously monitors at multiple points in both circuits of each coupon and records the data.

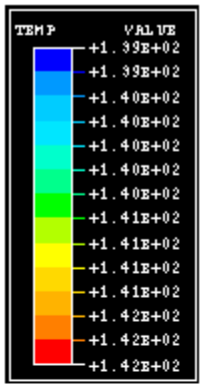
Example of Resulting Data Analysis



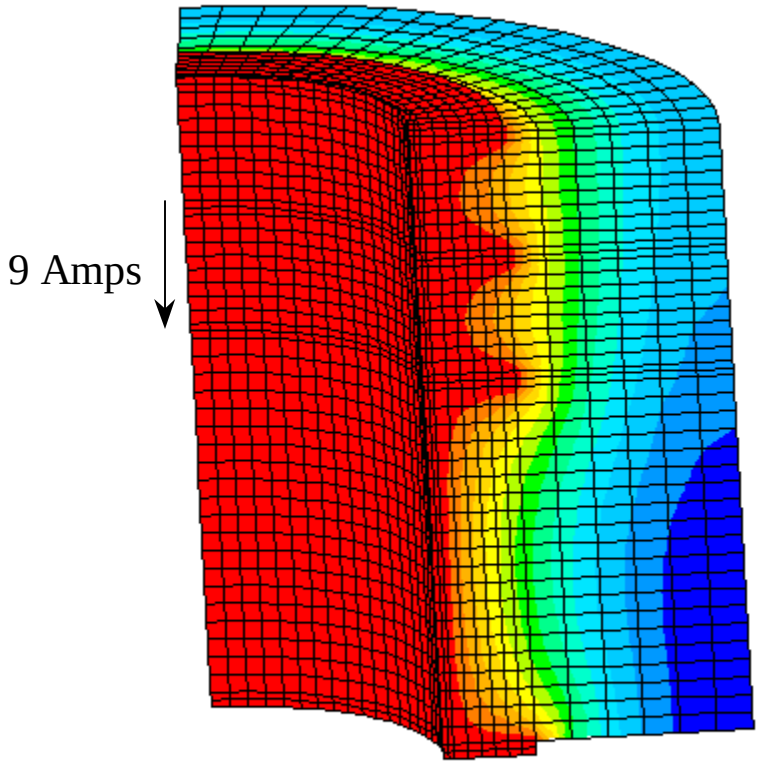
Post interconnection failure that starts to occur at 70 cycles while the barrel doesn't show signs of failure until 250 cycles.

Axisymmetric Electro-Thermal FEA of IST Coupon

(Current is equivalent to 9 Amps in Barrel Between Layers 2 and 3)



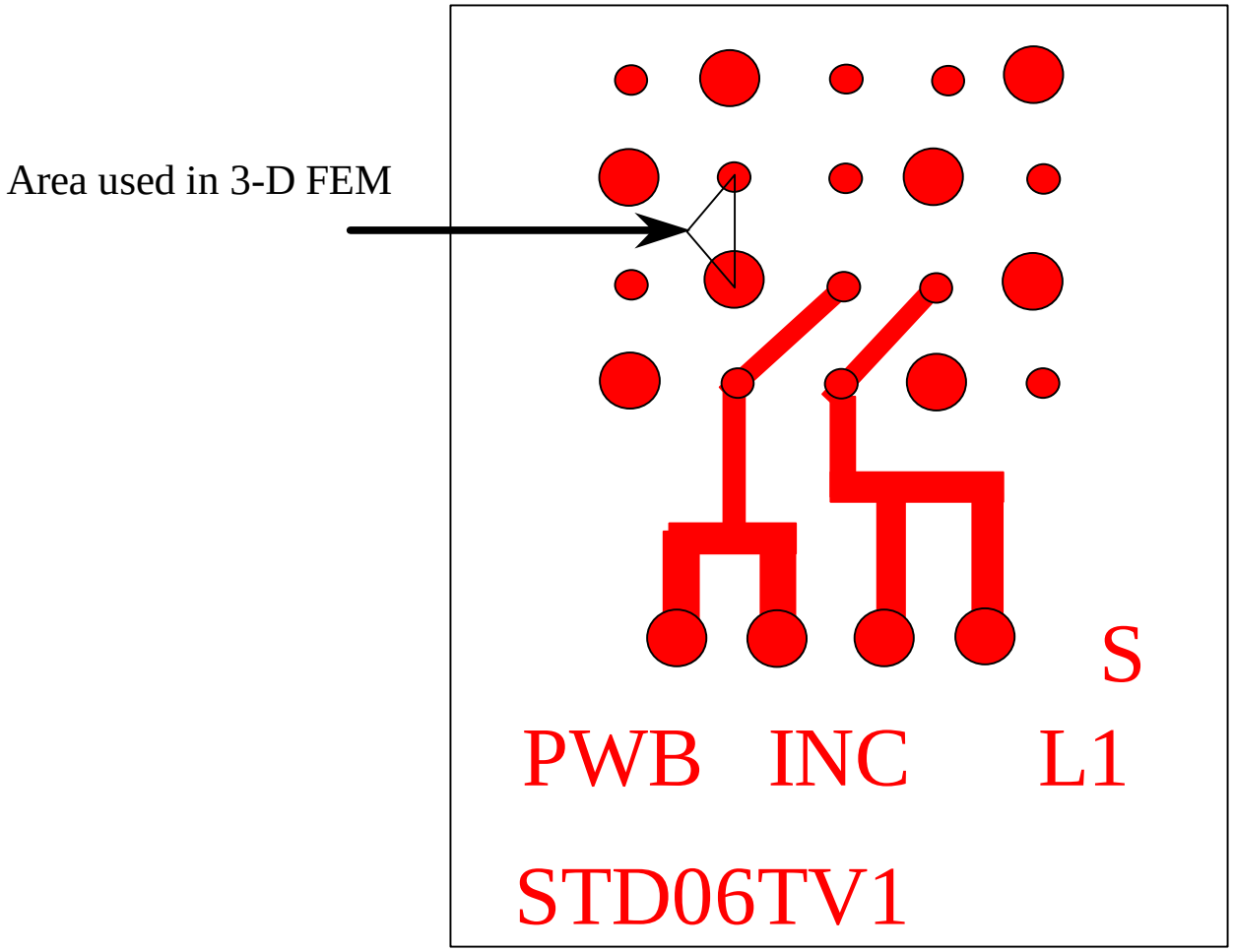
Maximum value = 142.0 at node 456
Minimum value = 139.1 at node 63



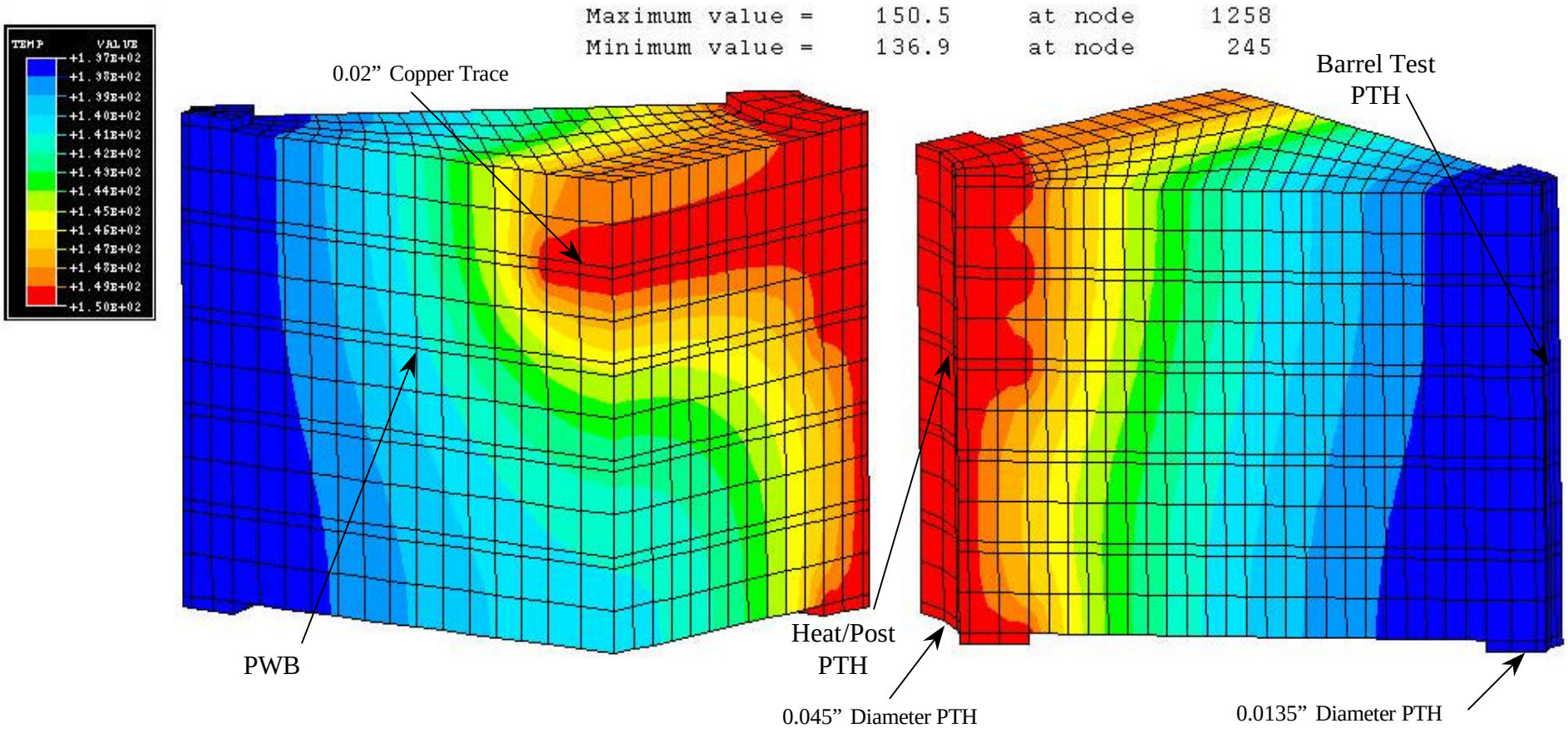
RESTART FILE = 6layer STEP 1 INCREMENT 180
TIME COMPLETED IN THIS STEP 180. TOTAL ACCUMULATED TIME 180.
ABAQUS VERSION: 5.7-1 DATE: 23-FEB-1999 TIME: 11:01:52

Section Taken for 3-D FEM

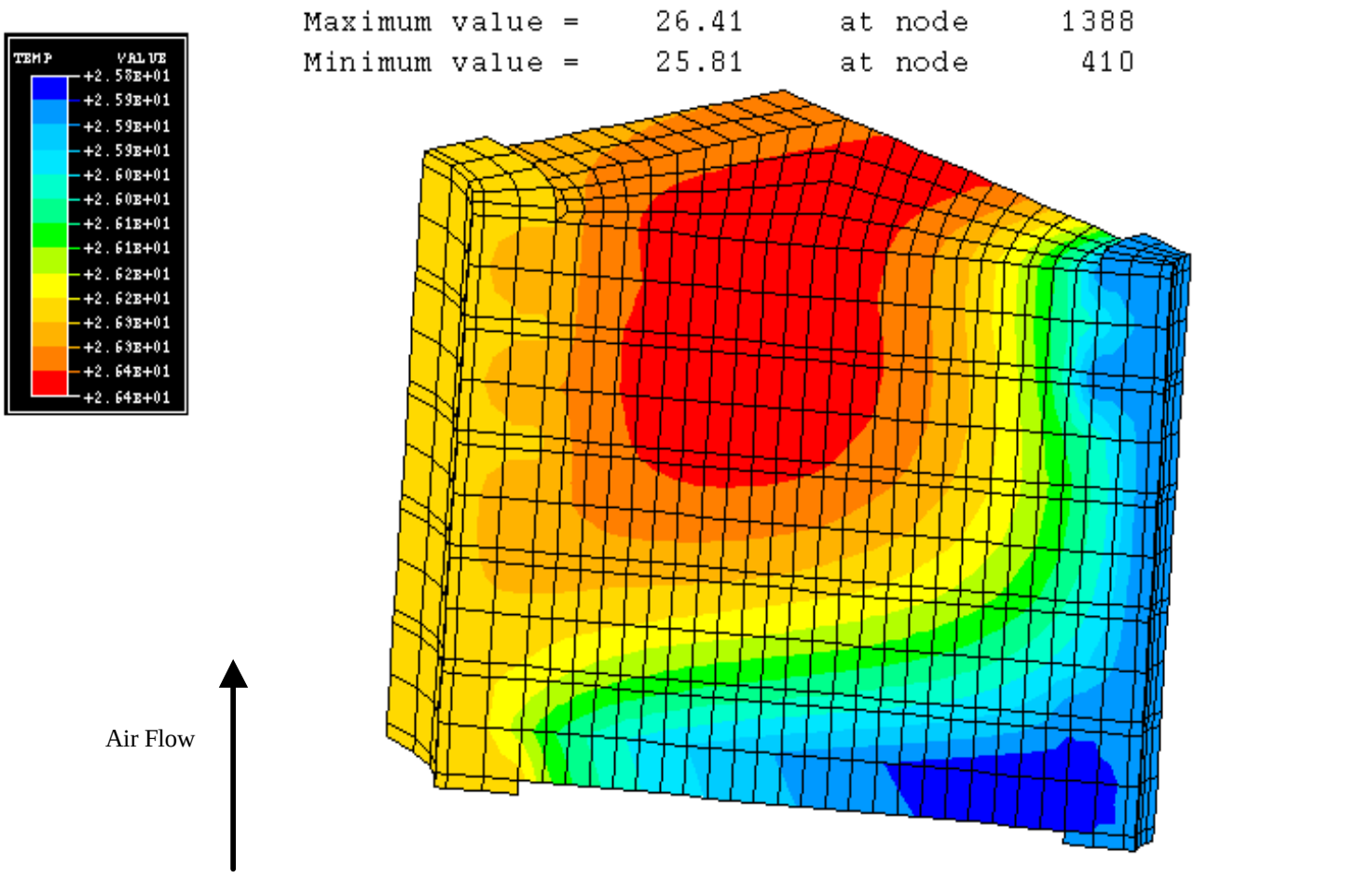
(Current Induced Heating Phase & Forced Convection Cooling Phase)



Temperatures After 3 Minutes Heating, 6 Layer PWB

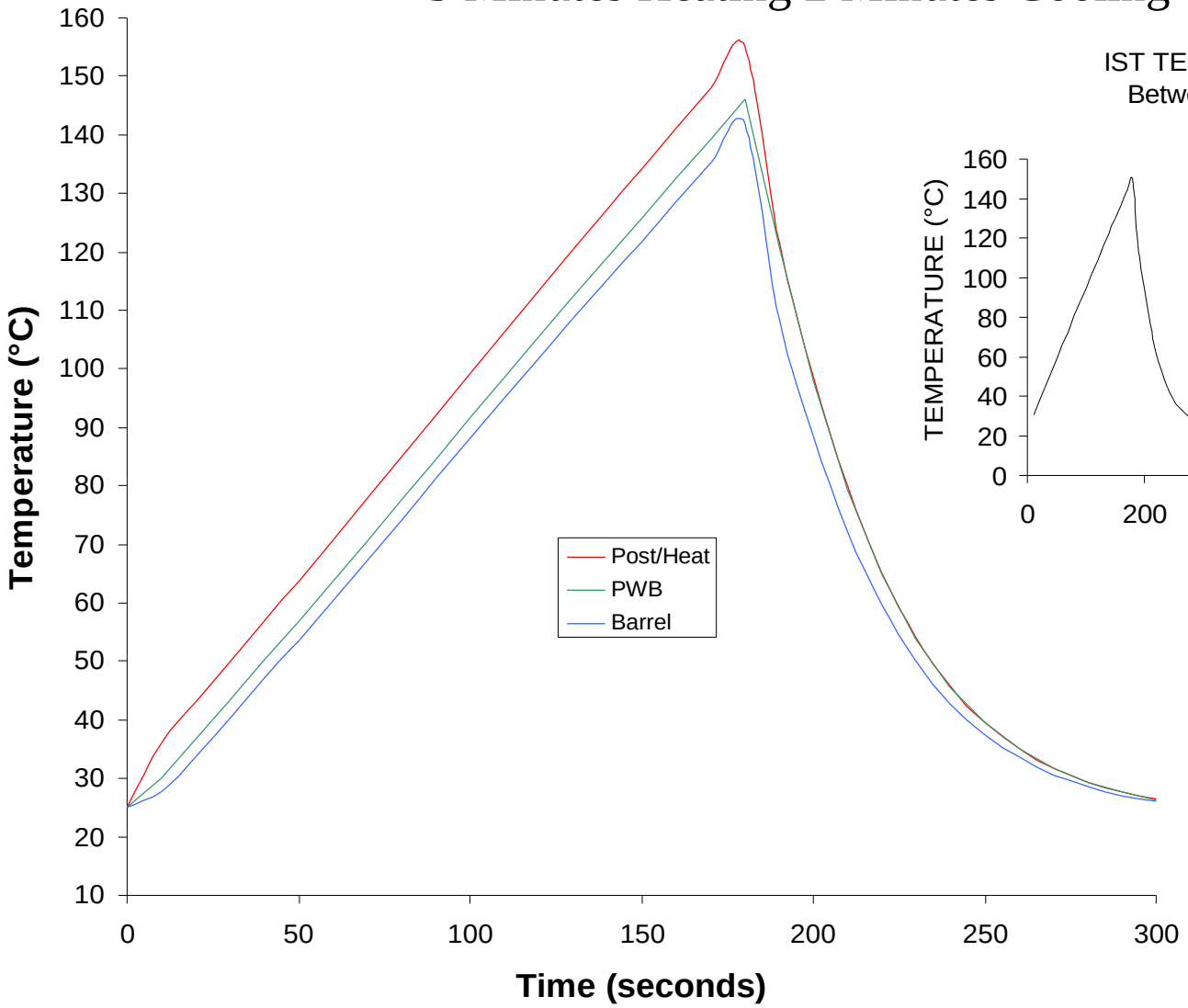


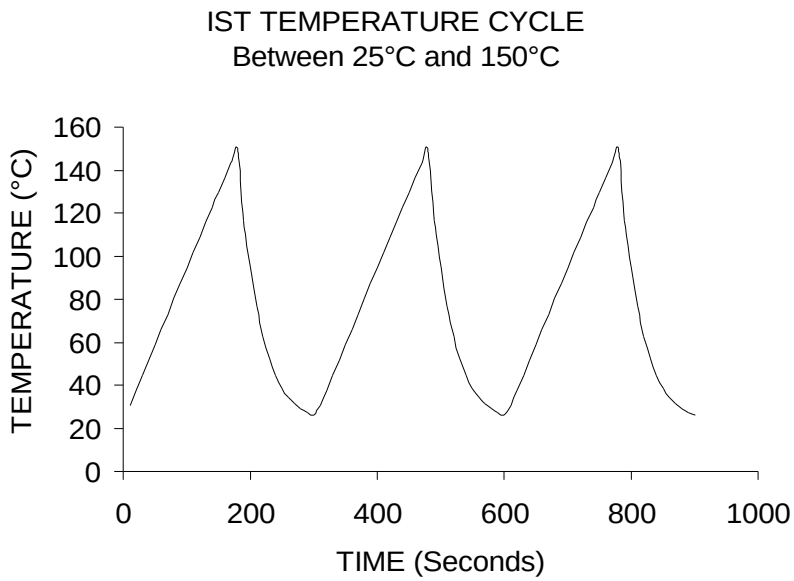
Temperature Gradients After 2 Minutes of Forced Air Cooling



Temperature Cycle Profile

3 Minutes Heating 2 Minutes Cooling





Conclusions From FEA

- Axisymmetric model is inadequate
  - more current required to heat the board using only vias
  - heating is primarily due to current in traces
- Board heating is thorough with small temperature gradients.
- Temperature increase is linear during heating phase.

Delphi Delco IST vs Oven Cycling Test*

(samples from same panel)

- IST test temperature ranges

  (3 minutes heating and 2 minutes cooling per cycle)

  - 25°C to 150°C
  - 25°C to 170°C
  - 25°C to 190°C

- Oven test temperature ranges

  (Dwell time of 20 minutes at each extreme)

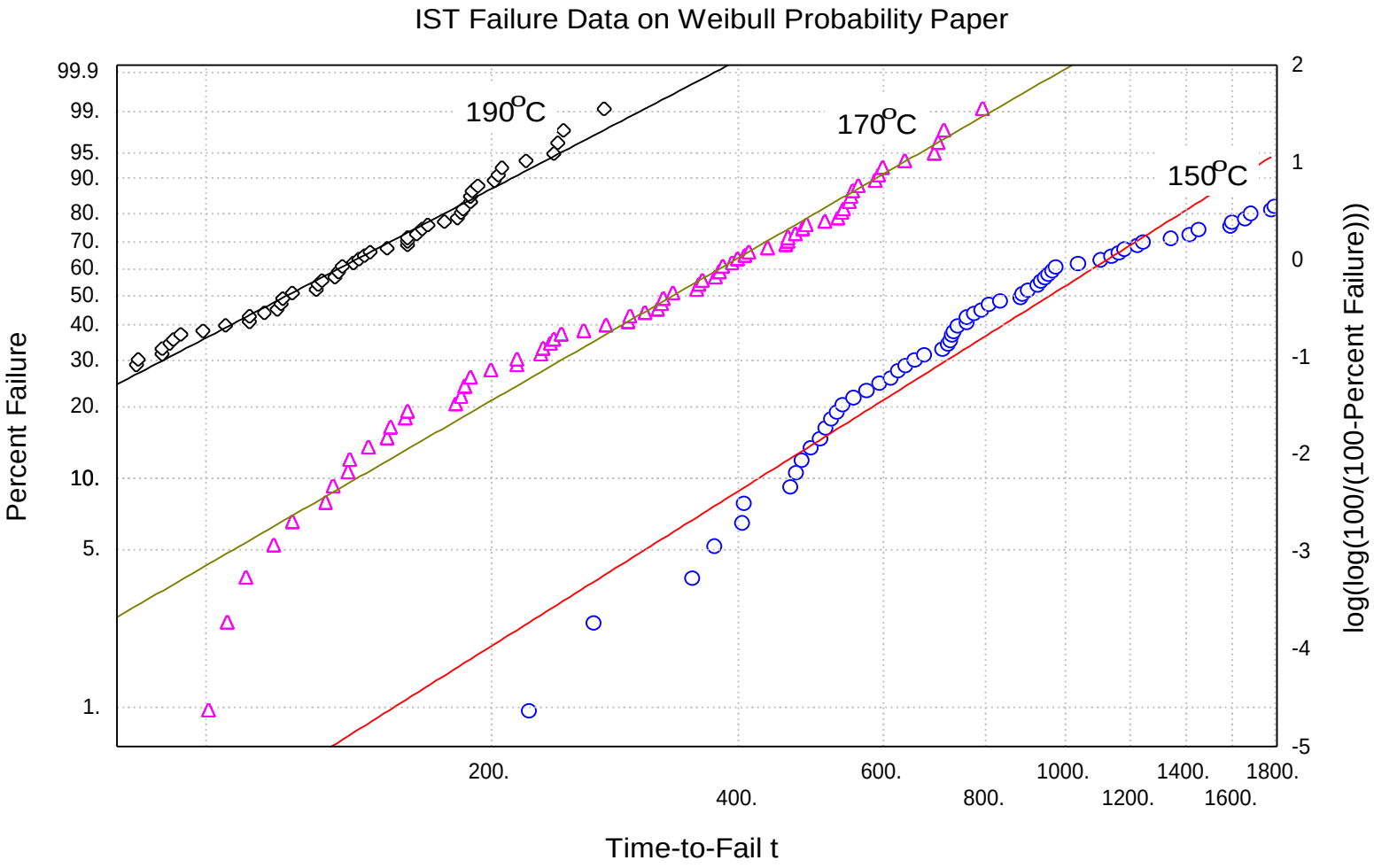
  (50 minutes per cycle)

  - -40°C to 125°C
  - -40°C to 145°C
  - -40°C to 165°C

** Available for download on web*

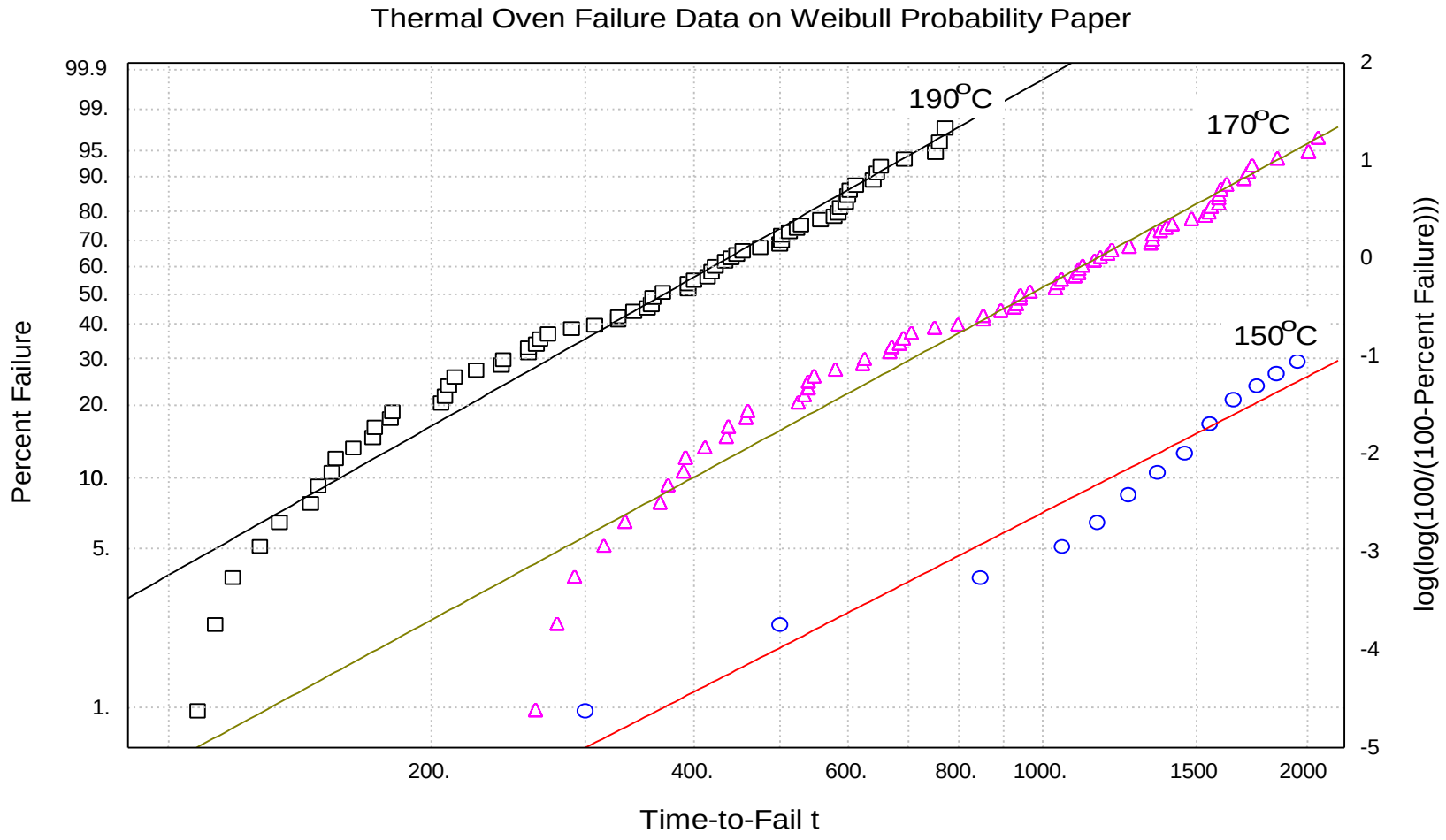
Delphi Delco IST Failure Data

NOTE: Data analyzed and presented wrt T_{max} not DT



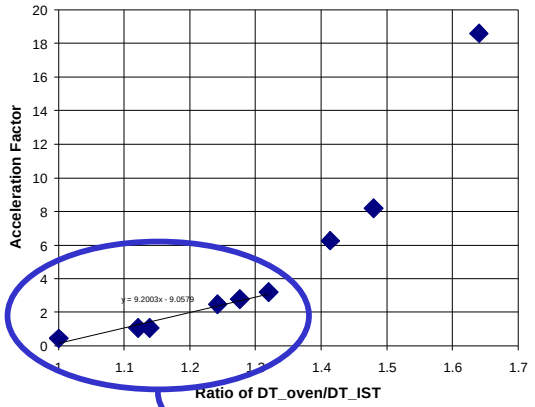
Delphi Delco Oven Cycling Failure Data

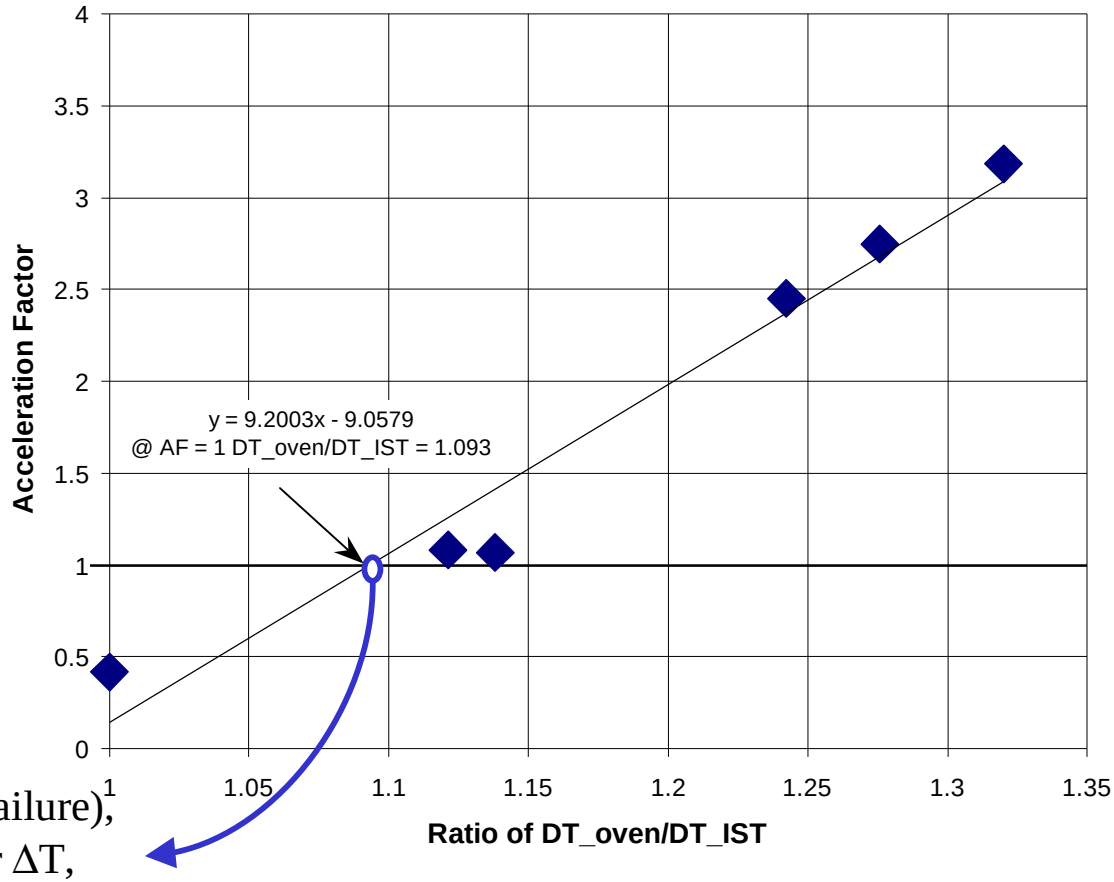
NOTE: Data analyzed and presented wrt T_{max} not DT



New Interpretation of Delphi Delco Data

(temperatures expressed in terms of DT)





$$AF = N_{IST} / N_{oven}$$

For AF=1 (same number of cycles to failure), oven cycling requires 1.1 times higher ΔT, i.e. IST test is slightly more severe.

Work Accomplished

- FEA model of IST coupon
- IST thermal transients and gradients not significant
- Preliminary Analysis of correlation data between IST and oven cycling imply that CALCE PTH model can be easily used to predict both IST test and field life using ΔT.

Work Remaining

- Locate additional IST and oven data for correlation studies
- Additional correlation studies using the CALCE PTH model with IST and oven cycling data
- *Investigate resin rich areas and correlation with IL separation using FEA*

PTV Interconnect Reliability Concerns

(in hierarchical order)

- *Thermal Cycle - (CALCE)*
- Copper plating thickness/quality, (uniformity, ductility, elongation, tensile strength).
- Material Tg, CTE, board thickness, hole diameter, number of layers (glass to resin ratio).
- Surface finish, PTH metallization, foil thickness, construction, grid size).
- Design (pads Vs no pads, annular ring, anti-pad clearance).

RE: Bill Birch, PWB Interconnect Solutions Inc.

(from personal and IPC Technet discussions)