Application of Reliability/Survival Statistics to Analyze Interconnect Stress Test Data to Make Life Predictions on Complex, Lead-free Printed Circuit Board Assemblies

Michael Freda
Sun Microsystems, Inc.
Menlo Park, California, USA

Jason Furlong
PWB Interconnect Solutions, Inc.
Ottawa, Ontario, CANADA

Abstract
Interconnect Stress Testing (IST) was developed during the 1990's as a test method for measuring plated through via and internal interconnect reliability in printed circuit boards. Historical results from IST testing on Sun's Enterprise Server Products will be discussed followed by data analysis results from the latest round of IST testing at Sun in support of our coming generation of lead-free servers. Of particular interest will be the introduction of a new data analysis methodology that allows prediction of plated through via cycles to failure versus the applied thermal stress temperature. This new method provides significant insight into plated through via reliability, accumulated fatigue damage, and plated through via life versus thermal stress temperature. After the PCB fabrication process and materials have been characterized, the new IST testing and data analysis method provides a clear understanding of the consumption of plated through via life during assembly and rework, the impact of lead-free processing versus eutectic solder, and the ability to predict the remaining life of products in the field.

Introduction
IST testing utilizes custom designed testing equipment that is used to measure cycles to failure (CTF) on specially designed IST coupons that are manufactured on the PCB fabrication panel. IST coupons are thermally cycled using ohmic heating (i.e., by an internal resistance heater circuit) on IST testing equipment until failure which is defined as a 10% increase in the resistance of a plated through via daisy chain. The IST test method (reference IPC-TM-650-2.6.26) has a number of advantages including: a quick cycle time of 5 minutes per cycle (≡288 cycles per day), the ability to precondition coupons on the IST equipment to simulate the thermal stress encountered at assembly, the capability to reach lead-free peak temperatures of 260ºC during preconditioning, and the ability to obtain quantitative data on plated through via cycles to failure.

This paper does not include a discussion or introduction to IST testing and/or IST coupon design. For detailed information on these topics visit the following web URL: www.pwbcorp.com.

Terms and Definitions
CI = confidence interval
CTE = coefficient of thermal expansion
CTF = cycles to failure
DOE = design of experiment
DPM = defects per million
IPL = inverse power law
IST = interconnect stress test
LGA = land grid array
MLE = maximum likelihood estimate
POST = refers to an inner layer to plated hole connection, on an IST coupon this refers to a daisy chain that goes from one inner layer to another inner layer making connections through the plated via; this coupon is sensitive to shear failure at the inner layer pad the plated hole interface
PTH = plated through hole, on an IST coupon this refers to a daisy chain that goes from top to bottom and can detect fatigue failures in the center of the plated via
SMT = surface mount technology

IST Testing History at Sun
Sun's first usage of IST testing was in 1998 during the early prototype development of the SunFire™ server product line. As introduced in 2001, this family of servers spans the range from 12 to 106 processors per system. Current SunFire™ server systems range from 24 to 212 processors.

The CPU board utilized in all the SunFire™ systems is 490mm x 420mm x 3mm, has 26 layers, utilizes buried via layer pairs, utilizes blind vias to layers 2, 3, 24, and 25, and uses mixed metallization with selective Cu/Ni/Au plating in the LGA socket area. Plated hole aspect ratios range from 8:1 to 9:1 depending upon the drilled hole size selected by the PCB fab supplier. The high layer count of 26 layers in a 3mm thick board results in a stack-up with thin dielectrics thickness and a high resin to glass ratio.

Early prototype IST testing by Sun used varying assembly precondition stresses of 0x, 3x, and 6x at 230°C followed by test to failure at 150°C. This testing showed that six assembly cycles consumes 50-80% of the via life. It was also quite common to see POST interconnect failures caused by the large Z-axis CTE expansion due to the high resin to glass ratio in the CPU PCB fab construction. The high Z-axis expansion results in a large shear stress on inner layer connections close to the top and bottom surface of the PCB fab. Through a close working relationship between the PCB fabrication suppliers,

PWB Interconnect Solutions, and Sun, these issues were corrected prior to product release.

During the years of 2001 through 2003 Sun continued to work with the PCB fabrication suppliers to baseline the via formation process on the SunFire™ product line and to continuously improve the CTF performance. It was during this time that Sun standardized on an IST testing protocol of 6x preconditioning at 230°C followed by test to failure up to a maximum of 500 cycles at 150°C. While Sun saw the average CTF value continue to increase over time due to process improvements at the PCB fabrication suppliers, the PCB fabrication supplier that had the highest CTF average was also most prone to early life failures. Due to this, in 2002 Sun switch to using a two-parameter Weibull distribution for CTF analysis. It is common practice when using the two-parameter Weibull distribution to report the characteristic life (i.e., 63.2% cumulative failure) and the slope. While characteristic life is the zero intercept of the Weibull mathematical transformation, it has little relevance to real life product reliability. For this reason, Sun uses T1% for its baseline data, i.e., the expected first failure from testing 100 IST coupons. To get high CTF results on the T1% metric, the PCB fabrication supplier must have both a good process (indicated by a high characteristic life) and a consistent process (indicated by a high slope).

In mid 2003 Sun switched from using a two-parameter Weibull analysis to using a Lognormal distribution. Although results from both analysis methods are similar, the Lognormal distribution has a better fit to the data in about 60% of the data sets analyzed and it has a better fit to early life failures which is Sun's primary interest.

In early 2004 Sun changed the testing protocol to allow our PCB fabrication suppliers on the SunFire™ program to test at 230°C to failure. This change was made after extensive testing at both 150°C and 230°C to failure. Data from this testing was then used to establish the acceleration factor between 150°C and 230°C CTF data. Once this acceleration factor is established, it allows the use of Miner's Rule[(1)] to predict cycles to failure to the pre-existing baseline that used the IST testing protocol of 6x preconditioning at 230°C followed by test to failure at 150°C. This change was made due to the large increase in CTF over time that resulted in long testing times to meet Sun's quarterly testing requirements. It seemed unfair to penalize the PCB fabrication suppliers for their process and product improvements that increased CTF performance but, also increased their testing time and cost for IST testing to failure. Similar to the concept of a "rational sample size" used in statistical process control, the better the via reliability process, the less value extensive testing provides.

Since Sun's original prototype IST testing in 1998 to today we have seen the T1% increase from low single digits values to today where all PCB fab suppliers exceed a T1% of 75 CTF on the SunFire™ product. During the production phase of this product we have gone from very low levels of via opens at assembly in the early production phase to today where a via open is rare. Throughout the life of the SunFire™ program there have been no reported failures for via opens in shipped product.

Testing Goals

There are a number of trends in electronics that resulted in the decision to perform the via reliability testing covered in this paper. Those major trends are:

- Regulations that eliminate the use of lead in electronic equipment including the eutectic tin/lead alloy. Switching to a SAC alloy (tin/silver/copper) results in a 30-35°C increase in peak assembly reflow temperatures.
- Increased signal speeds that require wider traces and thicker dielectrics to minimize attenuation loss but, result in thicker PCB fabs with higher aspect ratios.
- The use of large 2000+ pin, 1mm pitch, area array packages which require filled via in pad designs.
- Sun's desire to use CTF data obtained from testing combined with material properties to develop a predictive model of via reliability.

Test Panel Description

All data reported within this paper comes from testing on a 450 x 600 x 4mm panel that contains 18 daisy chain test coupons and 24 IST coupons. There are four IST coupon designs:

1. 300um drilled hole used for both the PTH and the POST interconnect daisy chain
2. 350um drilled hole used for both the PTH and the POST interconnect daisy chain
3. 350um drilled holes with the PTH daisy chain and 660um drilled holes with the POST interconnect daisy chain
4. 400um drilled hole used for both the PTH and the POST interconnect daisy chain

The panel thickness is 4mm resulting in hole aspect ratios of 13.1:1, 11.2:1, and 9.8:1. The panel is laid out so there are six groups of coupons. Within each group are three daisy chain coupons and four IST coupons, i.e., one of each IST coupon design. For the test results reported in this paper, only the IST coupons were used. Test results from the daisy chain coupons will be discussed in a separate paper. For a top view of the test panel see appendix 1.

Via Reliability Design of Experiments

The data used for the analysis performed in the remainder of this paper was obtained from testing on the PCB fab panel designed by Sun and PWB Interconnect Solutions and described in the preceding section. The test panel design plus material and process selections results in the following DOE conditions:

- 3x drilled hole diameters of 300um, 350um, and 400um.
- 4x IST coupon designs. In addition to the three drilled hole diameters listed where the same hole size was used in both PTH and POST daisy chains, the fourth IST coupon has both 350um PTH and 660um POST daisy chains.
- 2x plated hole conditions. One group of IST coupons used a standard plated through hole

process and the other group of IST coupons used a filled via in pad where the via is drilled, plated, filled, planarized, and then plated a second time over the fill material to create the via in pad configuration. Since each panel has both filled and non-filled vias, the processing sequence was changed from that used for a standard plated through hole process. Therefore, even the non-filled holes were subjected to this non-standard processing flow.

- 2x laminate materials. Both laminate materials used were aromatic phenolic cured epoxy glass, one with an inert filler to lower Z-axis CTE, the other without filler. Measured mechanical properties of the Lot 1 and Lot 2 materials (i.e., not obtained from data sheets) follows in Table 1.

IST coupons with the DOE variations listed above where then tested to failure at 130°C, 150°C, 170°C, 230°C, and 260°C.

Data Naming Conventions
The following naming convention is used for both raw data and analyzed data:

F = IST coupons with filled vias
N = IST coupons with non-filled via
1 = IST coupons from Lot 1
2 = IST coupons from Lot 2
xxxC = IST test temperature in ºC
yyy = designates an IST coupon design where the same drilled hole diameter (yyy in um) is used for both the PTH daisy chain and the POST interconnect daisy chain
350/660 = designates an IST coupon design where a 350um drilled hole diameter is used for the PTH daisy chain and a 660um drilled hole diameter is used for the POST interconnect daisy chain

Example 1 - F2/170C/350 refers to an IST coupon design with a filled via from Lot 2 where a 350um drilled hole size is used for both the PTH daisy chain and the POST interconnect daisy chain, IST testing was performed at 170ºC.

Example 2 - In tables and graphs of the IST coupon design versus temperature this name would be shortened to F2/350 since the temperature will now be shown in the other axis/column.

Laminate Material Properties
Prior experience at Sun has shown that the laminate material used is an important factor in via reliability. It is quite typical within the PCB fabrication industry to assume that plating quality is the main factor in via reliability. Nonetheless, it is Sun's experience that if you are using PCB fabrication suppliers with very good processes for drilling, cleaning of holes after drilling, and high quality plating, then the laminate material used becomes the primary factor in via reliability. Based on earlier testing at Sun, the laminate materials selected were both aromatic phenolic cured epoxy resin systems coated on electrical glass. Mechanical properties that were measured on Lot 1 and Lot 2 laminate materials follows in Table 1.

	Mechanical Parameter	Measured Data	Units
Lot 1	Tg by TMA	154.4	ºC
	Z-axis CTE < Tg	62.2	PPM/ºC
	Z-axis CTE > Tg	281	PPM/ºC
	TMA Tg transition	123-167	ºC
	Z-axis expansion, 230ºC	2.9	%
	Z-axis expansion, 260ºC	3.8	%
	Tg by DMA	167	ºC
	Storage modulus below Tg	16,400	MPa
	Storage modulus above Tg	600	MPa
	DMA Tg transition	145-185	ºC
	Laminate Description	aromatic phenolic cured epoxy glass laminate	
Lot 2	Tg by TMA	171.2	ºC
	Z-axis CTE < Tg	24.4	PPM/ºC
	Z-axis CTE > Tg	197.3	PPM/ºC
	TMA Tg transition	151-178	ºC
	Z-axis expansion, 230ºC	1.5	%
	Z-axis expansion, 260ºC	2.1	%
	Tg by DMA	172	ºC
	Storage modulus below Tg	16,400	MPa
	Storage modulus above Tg	900	MPa
	DMA Tg transition	155-190	ºC
	Laminate Description	aromatic phenolic cured epoxy glass laminate with inert filler to lower CTE	

Table 1 – Mechanical properties of the laminate material used in Lot 1 and in Lot 2.

For the IST testing reported on in this paper, only epoxy glass laminate materials were evaluated due to their wide use, high availability, and generally lower cost.

IST Testing Conditions
The typical IST test cycle involves a linear three-minute ramp from ambient to peak temperature. This heating is achieved through the use of an in-situ resistance heater circuit designed into the IST coupon. A computer controlled power supply provides current to reach the temperature peak. When the peak temperature is reached at the end of three-minutes, the power supply shuts down and a fan is switched on to cool down the IST coupon using ambient air for the next two-minutes. This cycle is then repeated...

For the testing at 230ºC and 260ºC the IST coupons where cycled between ambient at 230ºC (or 260ºC) until failure. For the testing at 130ºC, 150ºC, and 170ºC the IST coupons where first cycled two times from ambient to 260ºC followed by test to failure at 130ºC, 150ºC, or 170ºC. The reasons for performing these two preconditioning cycles are:

- It is thought that a high temperature exposure may effect and change the laminate materials. Therefore, not performing this preconditioning step may create misleading CTF results.
- Since Sun never ships bare PCB fabs to suppliers. All assembled product receives a

minimum of two assembly reflow thermal stress cycles.
- Because assembly thermal stress has a large effect on via life, performing this preconditioning shortens the CTF testing required at the lower temperatures.

Lognormal Data Analysis

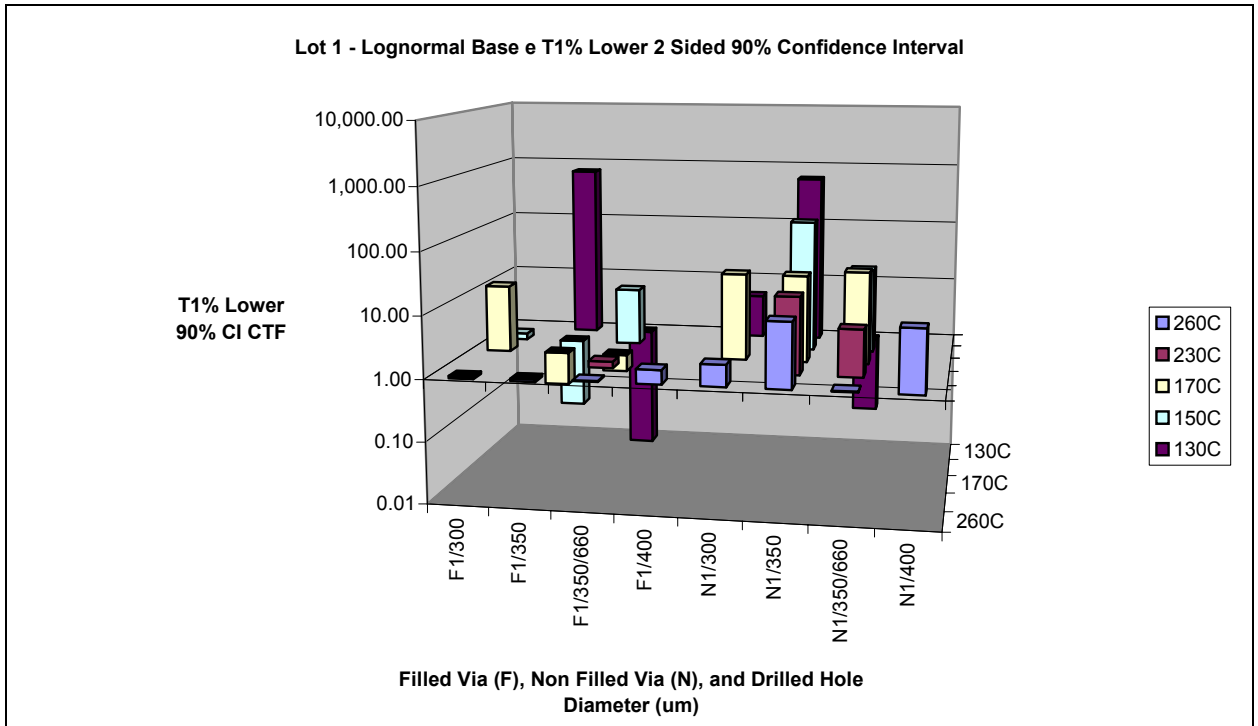
The initial data analysis was performed with Minitab release 13 using it's Lognormal base e MLE analysis. The T1% lower 90% two sided confidence interval results from this initial data analysis are summarized in Table 2. This same data is also used for the three-dimensional plots shown in Graph 1 and Graph 2.

The raw CTF data utilized for the Minitab Lognormal data analysis is attached in Appendix 2–5. Within each appendix, the first page contains the raw data and Lognormal base e MLE summary statistics followed by two pages of Lognormal plots. Each plot is for a given DOE cell (e.g., F1/300) with a separate Lognormal base e MLE plot for each IST test temperature within that DOE cell.

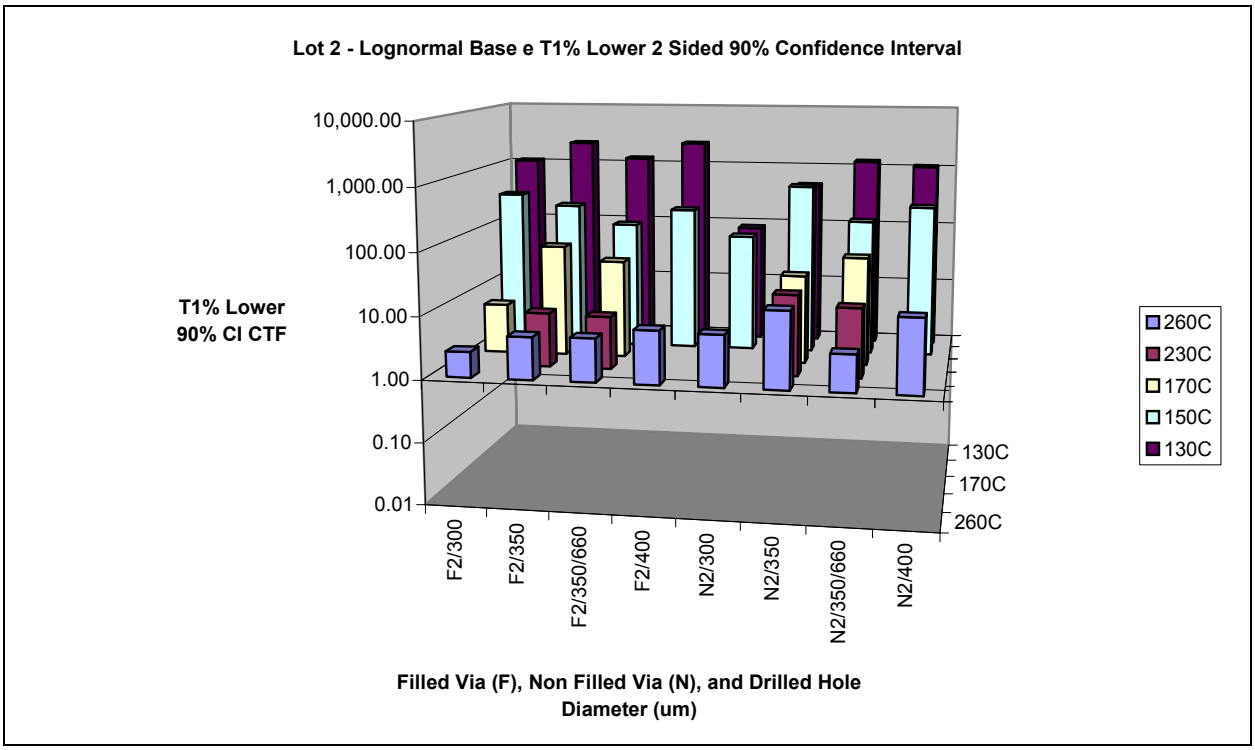
The plots in appendix 2-5 as well as Graphs 1 and 2 were used to select DOE cells for follow-on analysis using ReliaSoft ALTA Version 6 which is the topic of the remainder of this paper.

	IST Testing Temperature (degrees C)				
	260C	230C	170C	150C	130C
F1/300	0.920		12.5	1.26	
F1/350	0.910		0.294	0.077	695
F1/350/660	1.04	1.27	0.537	8.42	0.00003
F1/400	1.69				
N1/300	2.23		25.9		5.10
N1/350	11.2	17.8	25.7	143	598
N1/350/660	1.03	5.81	31.6	24.0	0.0585
N1/400	10.3				
F2/300	2.59		6.30	346	1079
F2/350	4.79	7.43	63.4	233	2287
F2/350/660	4.96	6.97	37.7	115	1262
F2/400	7.13			215	2374
N2/300	6.62			80.1	83.4
N2/350	16.8	19.5	26.5	579	480
N2/350/660	3.94	12.9	55.4	157	1268
N2/400	15.3			284	1069

Table 2 – IST CTF data for each DOE design variation versus testing temperature. Data shown is the T1% lower 90%, two sided confidence interval using a lognormal MLE analysis.



Graph 1 – Lot 1, filled vias are on the left side, non-filled vias are on the left side. Within each via type data runs from smallest hole on the left to largest on the right.



Graph 2 – Lot 2, filled vias are on the left side, non-filled vias are on the left side. Within each via type data runs from smallest hole on the left to largest on the right.

Review of Graph 1 shows that Lot 1 exhibited inconsistent results. Only the N1/350 data follows the expected trend where CTF consistently increases as the stress temperature is decreased. While failure analysis is still being performed, there appear to be a couple of contributing factors to the erratic results:

1. The Lot 1 laminate material had a noticeably higher Z-axis CTE compared to Lot 2.
2. An aggressive planarization process that removed the copper wrap around plating.
3. It also appears possible that the hole fill material has a large Z-axis CTE and "blows" off the plating over the top of the fill material that forms the via in pad structure.

Table 3 also shows the inconsistent IST CTF results on Lot 1. In this Table the scale factor from the Lognormal base e MLE analysis is listed. The scale factor indicates the consistency of the data set. A low scale factor indicates a consistent PCB fabrication process (including laminate material). Although the ranking here is relative to this DOE, the cells that are color coded in RED (the worst) and YELLOW (marginal) indicate the cells with high scale factors. Lot 1 contained all five RED cells and four of the seven YELLOW cells.

Photos 1-5 show microsections taken from a filled via and a non-filled via in Lot 1. It should be noted that IST testing is performed to failure therefore, even "good" vias with high CTF ultimately fail. Failure analysis of vias that fail early and comparison to vias with high CTF can be very informative.

	IST Testing Temperature (degrees C)				
	260C	230C	170C	150C	130C
F1/300	0.469		0.366	1.221	
F1/350	0.512		0.975	1.528	0.295
F1/350/660	0.191	0.562	0.745	0.365	2.873
F1/400	0.327				
N1/300	0.392		0.237		1.227
N1/350	0.086	0.024	0.220	0.185	0.242
N1/350/660	0.191	0.158	0.118	0.179	1.356
N1/400	0.131				
F2/300	0.366		0.578	0.277	0.214
F2/350	0.273	0.166	0.084	0.330	0.151
F2/350/660	0.091	0.153	0.179	0.467	0.210
F2/400	0.225			0.456	0.046
N2/300	0.319			0.513	0.723
N2/350	0.103	0.065	0.382	0.108	0.437
N2/350/660	0.379	0.051	0.120	0.382	0.166
N2/400	0.106			0.314	0.347

RED >= to 1.0	5 of 60	8%
YELLOW 0.5 to 1.0	7 of 60	12%
GREEN <0.5	48 of 60	80%

Table 3 – Scale factor from the IST CTF lognormal data analysis. A low scale factor value indicates a consistent process. The rating of RED, YELLOW, and GREEN is to allow an easy relative visual comparison of the process consistency within the data from this DOE.

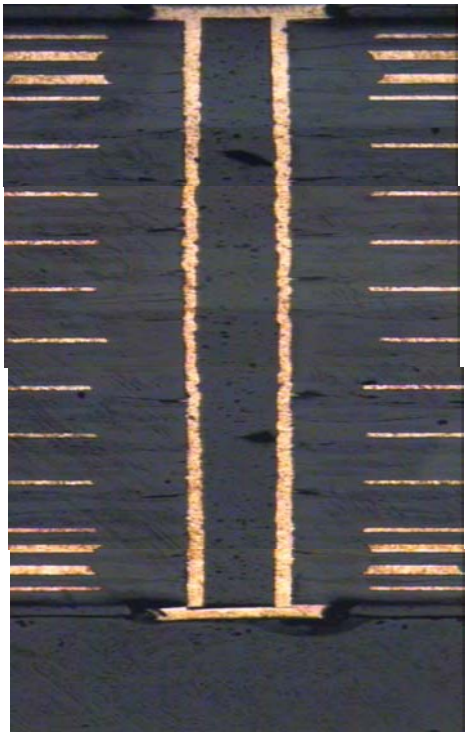


Photo 1 – Microsection of a filled via from Lot 1. Note the plating over the filled via at the top and bottom of the microsection to form the via in pad structure. Failure occurred during 2x preconditioning at 260°C.

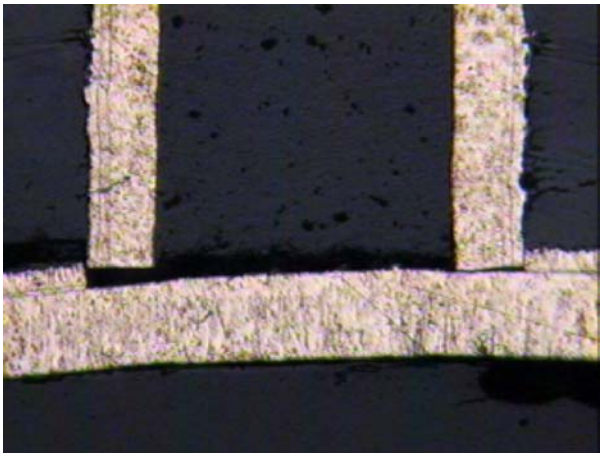


Photo 2 – Microsection of a filled via from Lot 1 enlarged to show the plating in and over the filled via in pad configuration.

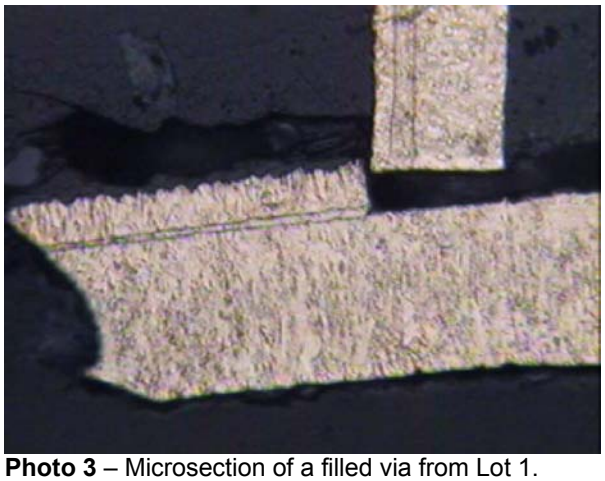


Photo 3 – Microsection of a filled via from Lot 1. Note the lack of copper plating wrap around at the corner due to aggressive planarization. This may be the cause of the early life failure of this IST coupon.

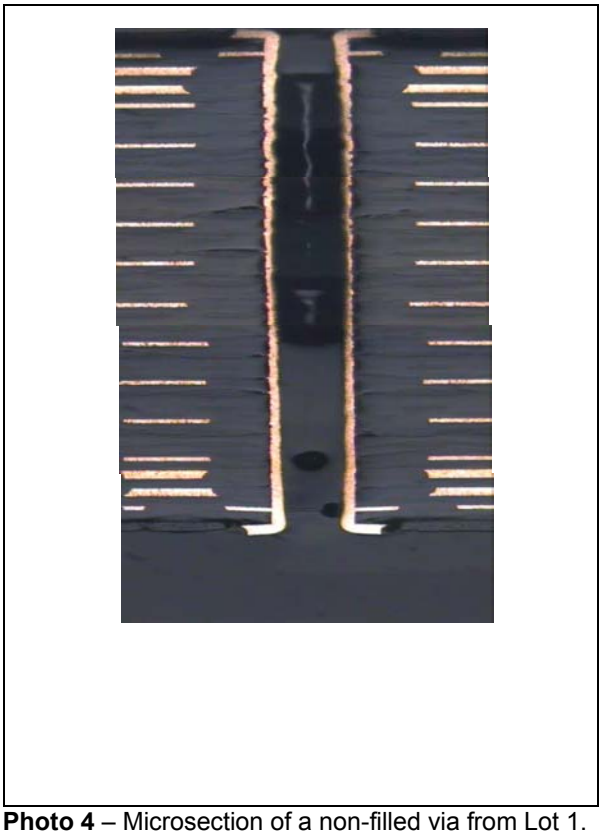


Photo 4 – Microsection of a non-filled via from Lot 1. Failure occurred after 2 preconditioning cycles at 260°C and followed by 792 CTF at 130°C.

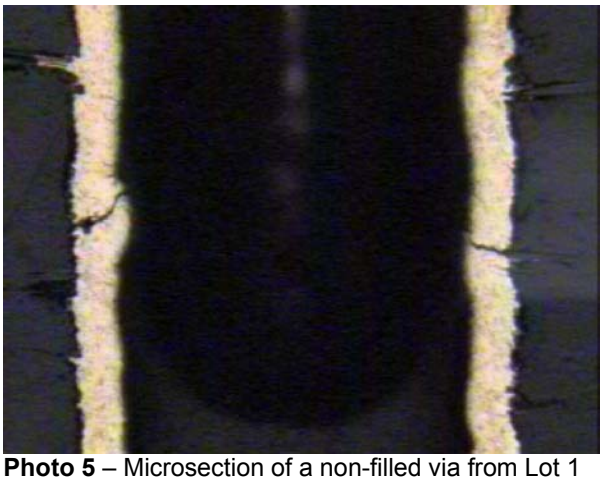


Photo 5 – Microsection of a non-filled via from Lot 1 showing a classic fatigue failure at high CTF.

Inverse Power Law Data Analysis

One of the goals of this DOE was to establish the CTF reliability of PCB fab vias versus applied thermal stress. This is one of the reasons that three temperatures were used for testing below Tg, 130°C, 150°C, and 170°C. Only a straight line can be drawn between two points; three are required to judge if the life-stress relationship under test is a good fit to the data.

During early life-stress data analysis using ReliSoft ALTA version 6, three life-stress relationships were tested: Arrhenius, Eyring, and Inverse Power Law. Actually, all three relationships had a relatively good fit. Nonetheless, the underlying basis of Arrhenius is thermodynamic and for Eyring is quantum mechanics therefore, the stress temperature used is degrees K. The difference between testing at 130°C (403°C) and 170°C (443°C) is only 10%. Quite simply, the narrow temperature range along with a relatively small sample size makes it difficult to ascertain if the data is a good fit to these life-stress relationships.

In discussions with the University of Maryland, CALCE[(2)] it was strongly suggested that the Inverse Power Law (IPL) be used as the life-stress relationship. Since there is a strong body of scientific knowledge to support the use of IPL in metal fatigue analysis and it was a good fit to the data (at least as good as Arrhenius or Eyring), IPL was used. IPL uses the temperature difference from high to low temperature extremes therefore, in this DOE the temperature induced stresses were: 108°C (e.g., 130°C - 22°C ambient), 128°C, 148°C, 208°C, and 238°C. This represents a 37% difference between the temperature induced life-stress at 130°C (a 108°C difference) and 170°C (a 148°C difference).

The mathematical relationship for IPL is[(3)]:

$$L(V) = \frac{1}{KV^{n}} \qquad \text{(eq. 1)}$$

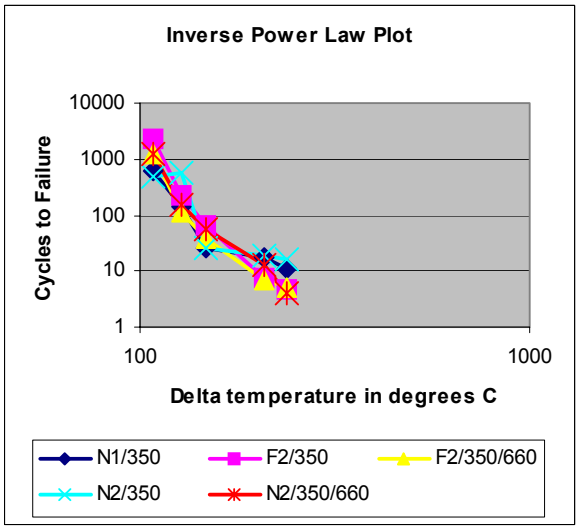
Where:

- **L** represents a quantifiable life measure, in the case IST cycles to failure
- **V** represents the stress level, in this case the temperature difference from IST peak temperature and ambient
- **K** is one of the model parameters to be determined, (K>0)
- **n** is another model parameter to be determined

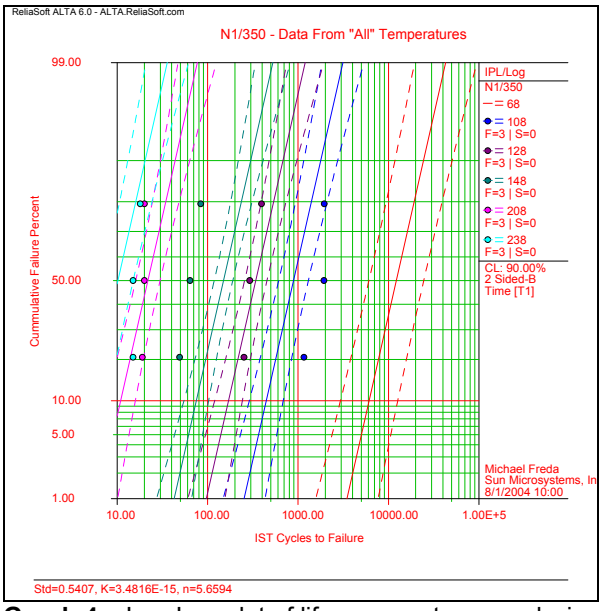
The IPL appears as a straight line when plotted on a log-log paper. The equation of the line is given by:

$$Ln\,(L) = -\,Ln\,(K) - n\,Ln\,(V) \qquad \text{(eq. 2)}$$

Graph 3 shows a simple Log-Log plot of five cells of the DOE that followed the expected trend and share a common 350um drill hole size. While this spreadsheet plot is crude, it shows that a straight line, IPL life-stress relationship, does not exist over the full temperature range. As expected, the slope above Tg does not match the slope below Tg.



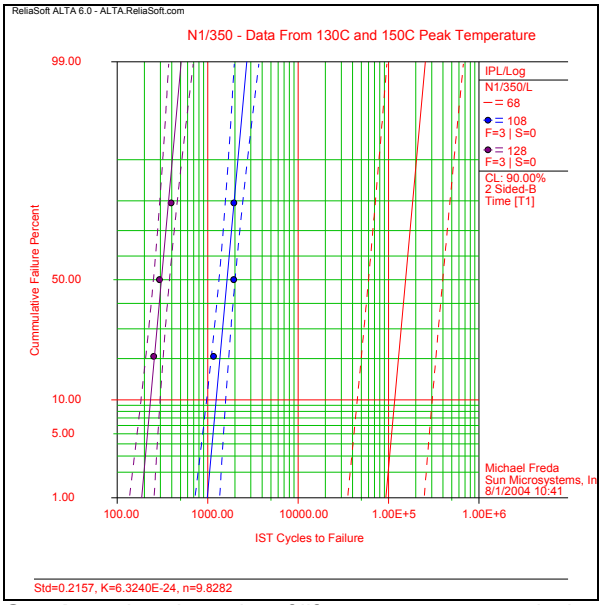
Graph 3 – Log-Log plot consistent with an inverse power law relationship. Note the upturn, i.e., lower slope above Tg. See Graphs 7-9 for more detailed plots of this data.



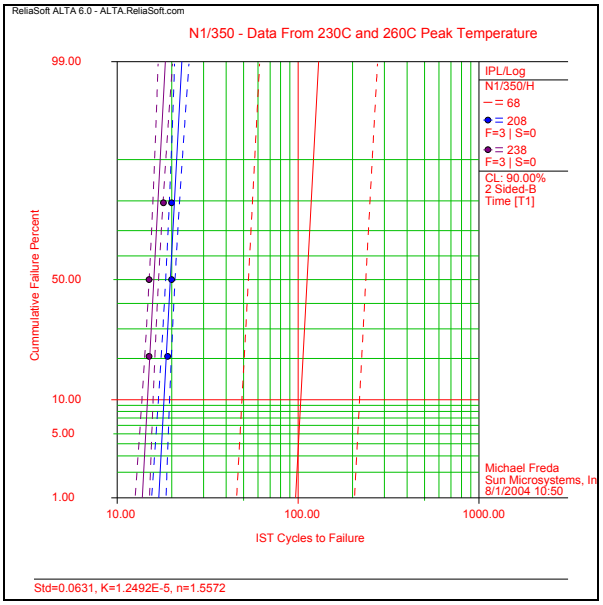
Graph 4 – Log-Log plot of life versus stress analysis using the inverse power law. All five testing temperatures used for this Graph.

Graph 4 is from an ALTA analysis of Lot 1, non-filled vias, with the 350um drilled hole size for both PTH

and POST daisy chain vias. This analysis used data from all five temperatures and does a Lognormal based e MLE best-fit with the same slope to each set of data. Additionally, it also uses equation 2 to determine a best-fit to parameters K and n to determine the IPL relationship. As can be seen, best-fit lines have a poor match to the data. This is a second confirmation that data above the Tg and data below the Tg needs to be analyzed separately. For the remainder of the data analysis only 130°C and 150°C data was used to analyze the life-stress relationship below Tg and 230°C and 260°C data was used to analyze the life-stress relationship above Tg. The data at 170°C was not used because it falls within the transition zone from glass to plastic state where CTE increases 5-6x and storage modulus decreases by 18-27x.



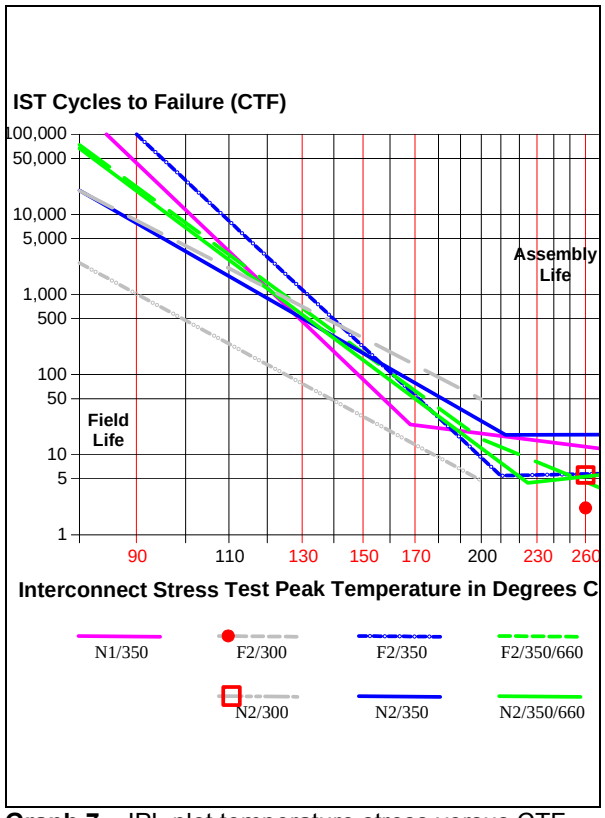
Graph 5 – Log-Log plot of life versus stress analysis using the inverse power law and only CTF data from testing at 130°C and 150°C, i.e., well below Tg.



Graph 6 – Log-Log plot of life versus stress analysis using the inverse power law and only CTF data from testing at 230°C and 260°C, i.e., well above Tg.

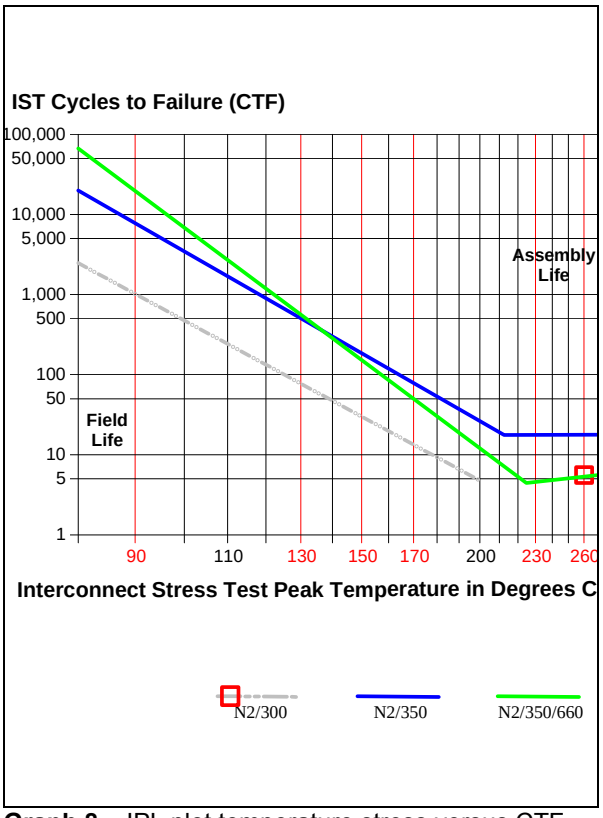
Graphs 5 and 6 include the same data as Graph 4 but, the ALTA analysis separates the data below Tg (Graph 5) and above Tg (Graph 6). This is the data analysis used for the life-stress graphs that follow. In both Graph 5 and 6, the solid red line is the estimated IST CTF at the stress temperature of 68°C which is equivalent to a peak temperature of 90°C (68°C difference + ambient 22°C). The dotted lines on either side represent the upper and lower two sided 90% confidence interval.

Graphs 7-9 show the combined IPL plots using data from ALTA including CTF below and above Tg. These plots are rather conservative in that they use the lower two sided 90% confidence interval. With the fairly small sample size used, typical six samples per cell, the confidence interval is quite large. Nonetheless, the strong temperature stress versus CTF is clearly seen below Tg. Between 230°C and 260°C the relationship is less clear.

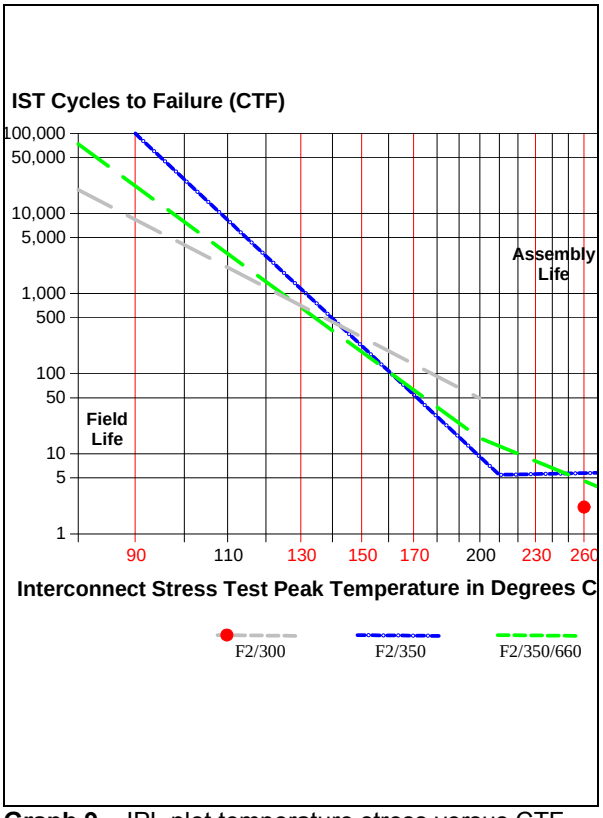


Graph 7 – IPL plot temperature stress versus CTF. N1/350, F2/300, F2/350, F2/350/660, N2/300, N2/350, and N2/350/660 data plotted.

Sun will be performing further testing to increase the sample size and therefore the statistical validity of the data. It should be noted the ALTA analysis assumes the same slope at the two stress temperatures and yet, the Lognormal plots in appendix 2-5 show this may be a bad assumption, especially for the high temperature testing at 230°C and 260°C. At these higher test temperatures the scale factors appear to be more stable but, the intercept (either T1% or mean life of T50%) is more variable. This makes predicting the CTF versus temperature inducted life-stress more difficult with small sample sizes.



Graph 8 – IPL plot temperature stress versus CTF. Only Lot 2, non-filled via data, i.e., N2/300, N2/350, and N2/350/660 data plotted.



Graph 9 – IPL plot temperature stress versus CTF. Only Lot 2, filled via data, i.e., F2/300, F2/350, and F2/350/660 data plotted.

Nonetheless, from this first round of lead-free testing at 260°C it appears that we could perform PCB fab assembly and still retain 60% or more of the via life.

For most DOE cells this represent >3,000 cycles in the field at a high 90°C peak temperature. Future testing of process improvements, especially on the hole filling process, improved laminate materials, and a larger sample size to reduce confidence interval width should result in improvement in these numbers.

Conclusion

There are a number of important observations from the IST testing and data analysis discussed in this paper:

1. The new IST testing protocol of testing to failure at multiple temperatures along with a change in data analysis methods provides much more insight into via life versus temperature stress.
2. Lead-free assembly temperature stress on thick PCB fabs vias that use epoxy glass laminate materials leaves little margin for error during assembly processing.
3. Rework, if allowed will need to be carefully controlled since every rework involves two thermal cycles, one to remove the old component and second to place the new component.
4. PCB assemblies that survive the thermal stress at assembly have a long life at field use temperature stress.
5. The hole fill process can result in a processing sequence that can adversely effect the reliability of non filled holes when both filled and non filled holes are combined on the same PCB fab panel.
6. There was a low level of failures due to POST interconnect separation (8 of the 278 coupons test with 7 of 8 at 260ºC). This failure mode is rarely seen on high aspect ratios vias at lower temperatures IST testing. Therefore, this failure mode needs to be watched carefully in future IST testing.

Future Work

Sun is plans to continue the work presented in this paper with the following activities:

- There are 18 daisy chain coupons per panel that represent a 2401 pin, 1mm, area array package. That daisy chain includes both filled vias and non-filled vias and three drilled hole diameters: 300um, 350um, and 400um. Sun plans to measure the via resistance of all 691,488 vias with a moving Kelvin 4-probe tester followed by thermal stress at a 260°C peak temperature in a standard SMT tunnel oven followed by retest. It is hoped to get DPM data for the number of thermal stress exposures versus drilled hole diameter.
- Continue our work with the University of Maryland, CALCE group to share Sun's IST and daisy chain testing data combined with basic materials testing to refine the CALCE via reliability predictive model.
- Continue to work with Sun's PCB fabrication suppliers and the laminate supplies to develop more robust PCB fabrication process and epoxy glass based laminate materials suitable for thick PCB fabs at lead-free assembly thermal stress conditions.

Acknowledgements
This effort was sponsored by Sun Microsystems with funding and technical input provided by David Towne, Derek Tsai, Tai Quan, Karl Sauter, and Charlotte Stoutamire. This work would not be possible without the equipment and technical knowledge of the personnel at PWB Interconnect Solutions, especially Bill Birch and Neil Copemen. The University of Maryland, CALCE staff, in particular Don Barker, Ph.D. and Craig Hillman, Ph.D. have supplied valued inputs on failure/fatigue models and materials properties. None of this work would be possible without the commitment to process improvement from Sun's high end PCB fab suppliers: Multek, Böblingen, Germany; Sanmina, Owego, NY; and Viasystems, Echt, The Netherlands and the active use of IST testing at EM supplier Celestica, Toronto, Canada. And last, special thanks to Carol Freda and Sharon Lutz, Ph.D. for their constructive review of this paper.

Michael Freda, Interconnect Specialist – *Sun Microsystems, Inc., Scalable Systems Group, Central Engineering, 15 Network Circle, UMPK15-103, Menlo Park, CA 95037, USA (Michael.Freda@Sun.COM).*
Mr. Freda has over 25 years experience in the electronics industry with the majority of that experience working in PCB fabrication. He has worked in start-up companies, at major OEMs, in the semiconductor packaging industry, and in semiconductor substrate fabrication in jobs ranging from product/process development, Engineering Management, Manufacturing Management, and Marketing. Mr. Freda has a BS in Applied Mathematics and Chemistry (ACS) from the University of Wisconsin and a MBA from the University of Minnesota. Mike currently works at Sun Microsystems supporting Sun's high-end server systems where he has been awarded five patents and has four patents pending.

Jason Furlong, IST Systems Engineer – *PWB Interconnect Solutions, Inc., 235 Stafford Road West, Unit 103, Nepean, Ontario K2H 9C1, Canada (Jason.Furlong@pwbcorp.com).* Mr. Furlong has three years experience in the electronics industry with the majority in IST Technology, product development, and statistical analysis software. Mr. Furlong has a Bachelors Degree in Electrical Engineering from the Memorial University of Newfoundland, Canada.

References
(1) J.E. Shigley and C.R. Mischke, 1989, "Mechanical Engineering Design, Fifth Edition," McGraw-Hill Book Company, pages 309-311.
(2) Don Baker, Craig Hillman, et al, 12 May 2004, Meeting at University of Maryland, College Park, MD.
(3) "Inverse Power Relationship Introduction," at www.weibull.com/AccelTestWeb/inverse_power_law

Reviewers

Sun Microsystems
Derek Tsai
Karl Sauter
Nyles Nettleton
David Love
David Towne
Dennis S.
Hank Ching
Keith Newman
CharLotte S.
Srirama Reddy
Frank Alberto

U of MD, Calce
Don Barker, Ph.D.
Craig Hilman, Ph.D.
Mike Pecht, Ph.D.

PWB
Neil Copeman
Bill Birch
Jason Furlong

Suppliers
Markus Siewurth
Tom Kopf
Rob van Pol
Joan Tourne

Family
Carol Freda
Sharon Lutz, Ph.D.