LAYER			
SIG	PLN		CU
●	01		1.0
	02	●	1.0
	03	●	1.0
	04	●	1.0
	05	●	1.0
	06	●	1.0
●	07		1.0
	08	●	1.0
●	09		1.0
●	10		1.0
	11	●	1.0
●	12		1.0
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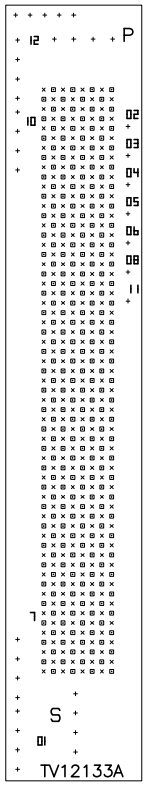
REV	DESCRIPTION OF CHANGE	DATE	ENG
A	ORIGINAL ISSUE	OCT 23 2014	JG

COPPER MUST BE LEFT IN THESE AREAS ON ALL LAYERS AND BE ROUTED THROUGH TO ALLOW EXPOSED COPPER ON EDGE/SIDE OF FINISHED PRODUCT



This drawing is for IST coupon information only
Coupon to be manufactured in accordance with the customer drawing
Coupon locations —within one inch of circuit pattern
—greater than one—half inch from panel edge
See readme.txt for PWB INC. contact information and other details
All files "Viewed from top"
All artworks are produced in a 'POSITIVE' polarity L2,3,4,5,6,8,11 are 'NEGATIVE'
See layer bar to identify specific product construction
All soldermasks are supplied 1 to 1 and should be adjusted as necessary
All drill data is contained in one file (see drill graphics)
All holes are plated unless otherwise specified
See drill table for tool/layer assignment ['SDL'=Start drill layer, 'EDL'=End drill layer]

Layers:	12
Coupon size:	.700 x 4.000
Grid spacing:	.050
Nonfunctional pads are:	Present
Hole/Pad:	.011/.023

This design is property of PWB Interconnect Solutions Inc.
Modifications to be approved by PWB Interconnect Solutions Inc.

**** .043 MUST BE DRILLED .043 (1.1MM or #57 DRILL)

FILE	SYM	TOOL	DHS	FHS	QTY	SDL	EDL	CKT
ncd	D310 +	T1	.043	****	36	1	12	CON
ncd	D320 ×	T2		.011	244	1	12	P1
ncd	D330 ▫	T3		.011	244	1	12	S1

PWB Interconnect Solutions Inc.
Ottawa, Ontario, Canada.
WWW.PWBCORP.COM (613) 596-4244

Title: INTERCONNECT STRESS TEST COUPON

Number	Rev	Size
TV12133	A	A

Filename: TV12133A.ZIP

Date: OCT 23 2014 | Sheet 1 of 1